A Low-Cost, 60GHz Driver Amplifier Operating from a Single +3V Supply

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Abstract

This paper describes the design and development of a low cost driver amplifier covering 57 to 64GHz. The IC is realised on a low cost GaAs PHEMT process produced on 6" diameter wafers with optically defined gates. It is a two stage design operating from a single +3V supply, drawing 36mA of current with 9dB gain and an output power (P-1dB) of over +13dBm. At the time of writing the IC is in fabrication. It is hoped that measured results will be available for the presentation. The paper includes details of the design procedure, the layout and the simulated performance including EM simulation of all matching and biasing networks.

Introduction

Large amounts of spectrum at around 60GHz are available on an unlicensed basis in many countries around the world [1]. The largest allocation is in the US where 7GHz of spectrum (from 57 to 64GHz) is available without any channelization requirements. One of the prime applications for this spectrum is short-range high-data rate links for WLAN. An amendment to the 802.11 WLAN standard (IEEE 802.11ad) will provide for data rates of up to 7Gbps in the 60GHz band.

The purpose of the development described in this paper was to realise an amplifier giving reasonable gain and >10dBm output power across the 57 to 64GHz band for potential use as an output driver for low power Si transceivers. One essential requirement for successful use in this application is low production cost. To help achieve this a low cost GaAs PHEMT process available on a commercial foundry basis through TriQuint Semiconductor was selected. The process features optically defined 0.13μm gates and is fabricated on 6" diameter wafers. Operation from a single +3V supply was also desirable and this feature was included in the design.

Design

At high mm-wave frequencies the available gain of transistors drops as device size (unit width and number of fingers) increases. Achieving a reasonable output power level and adequate gain is a challenge [2]. Operation from a single positive supply further exacerbates this problem. Single supply operation of depletion mode HEMTs requires the source to be floated by passing the drain-source bias current (Ids) through a resistor. This resistor is by-passed with a capacitor to provide a low impedance RF path. However, at mm-wave frequencies the parasitic inductances associated with the by-pass capacitor can start to have a significant effect on the RF performance.

Figure 1 is a plot of the Maximum Available Gain (MAG) of a 6 x 20μm transistor versus RF frequency as the source grounding inductance is varied between zero and 100pH in steps of 25pH. This was the transistor size used as the amplifier's output stage; bias was set to 2.8V Vds and 23mA Ids. It is clearly evident that high frequency gain is severely compromised by even modest amounts of grounding inductance. It can also be seen that one of the effects of modest levels of source inductance is to move the transistor from a region of unconditional stability back to a region of conditional

stability at higher frequencies. This is discussed in more detail in [2] but the effect of operating in a conditionally stable region is that gain must be sacrificed to stabilise the transistor.
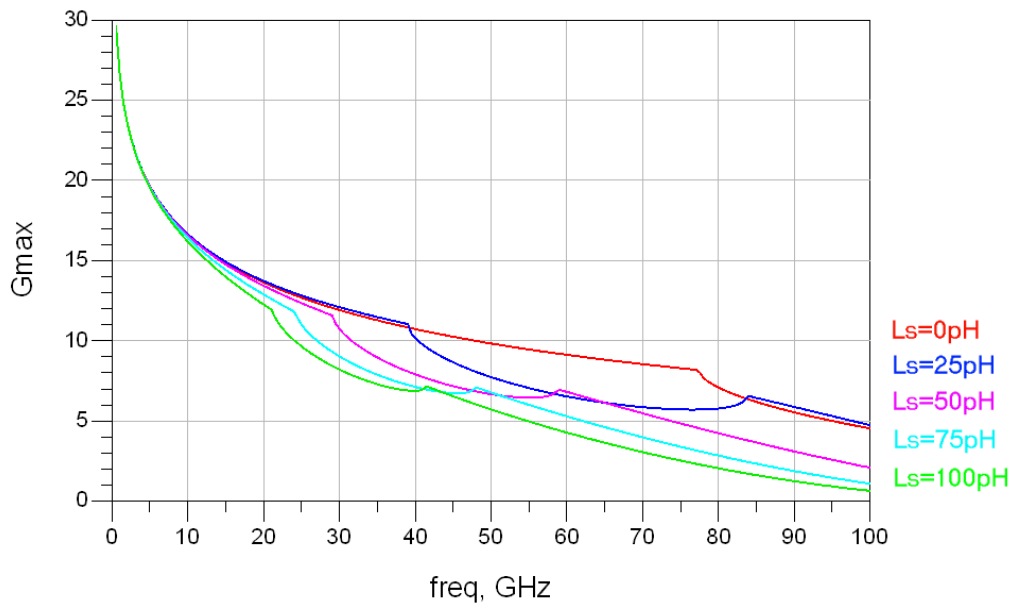
**Figure 1: Simulated transistor MAG versus frequency as grounding inductance is varied**

In actual fact the source inductance of the transistor cannot be reduced to zero. The equivalent inductance of two parallel vias with short interconnect lines to the transistor's source is 12pH. This then represents the minimum grounding inductance. The blue trace in Figure 1 represents 25pH of grounding inductance. In this instance the MAG at 60GHz is 7dB. With a self-biased transistor the parasitic inductance of the bypass capacitor augments the grounding inductance. Any additional parasitic inductance in the by-pass capacitors must therefore be minimised, which resulted in the development of the self-bias layout arrangement of Figure 2. The length of the by-pass capacitor is short to minimise its effective inductance and the width is wide enough to realise the required value of capacitance.
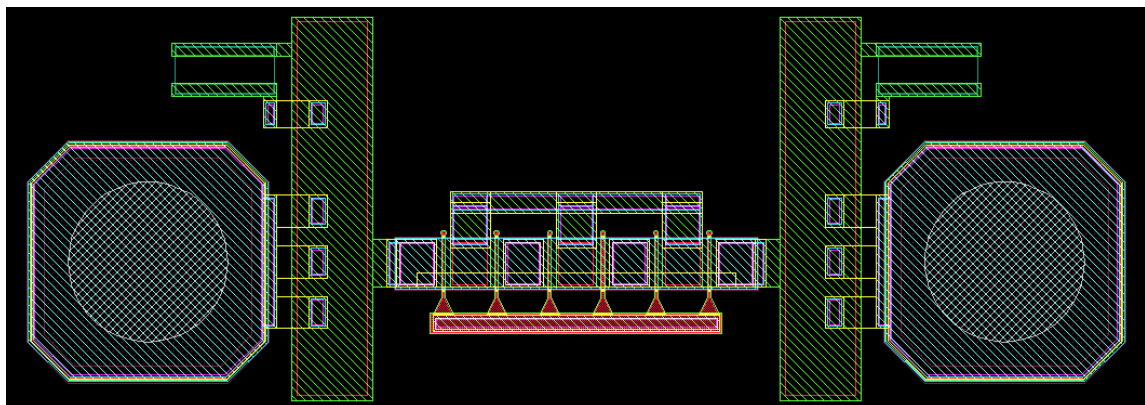
Figure 2: Layout plot of the output transistor with self biasing arrangement

The TQP13 process is actually a semi-enhancement process and a small positive gate-source voltage of around 0.25V was required. Whilst this offered the option of direct gate voltage bias using a potential divider from the single positive supply, this approach would result in higher unit to unit bias point and performance variation. The inclusion of a self-bias source resistor helps to stabilise the bias point and should also lead to reduced performance variation with temperature.

A 6 x 20µm transistor was selected as the output device and a 4 x 16µm as the input device. The smaller input device has much more available gain but less output power. The MAG versus frequency for each of these transistors, including the self-bias resistors and by-pass capacitors, is plotted in Figure 3. The red trace is the stage 1 transistor and the blue trace the stage 2 transistor. It can be seen that at 60GHz the stage 2 transistor has around 7dB of available gain and the stage 1 transistor almost 9dB. However, for the stage 1 transistor 60GHz is close to the point where the transistor transitions to a region of conditional stability and it was ultimately necessary to sacrifice a little gain to ensure stability close to band.
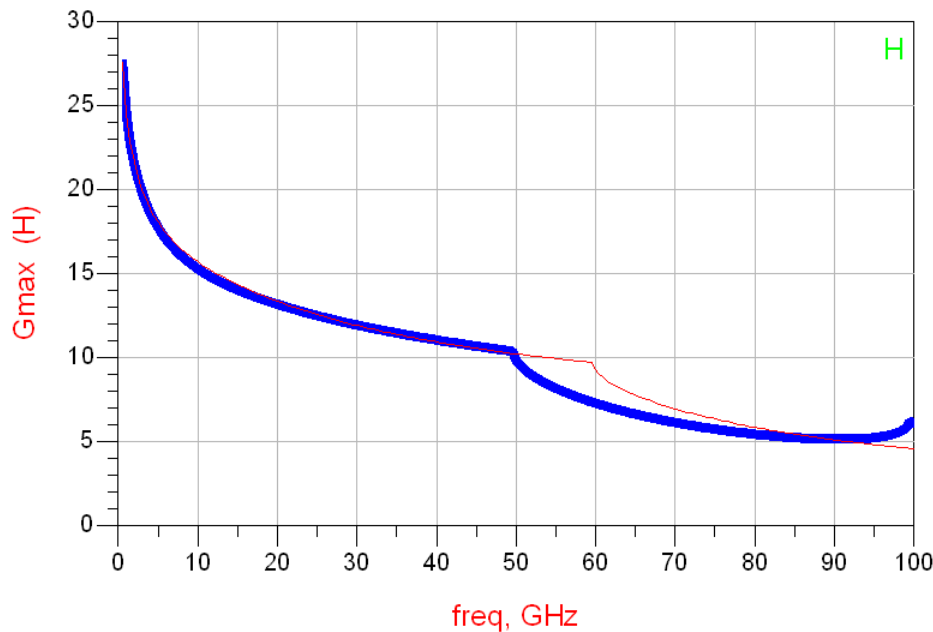
Figure 3: Gmax versus frequency of stage 1 and stage 2 transistors with self bias network
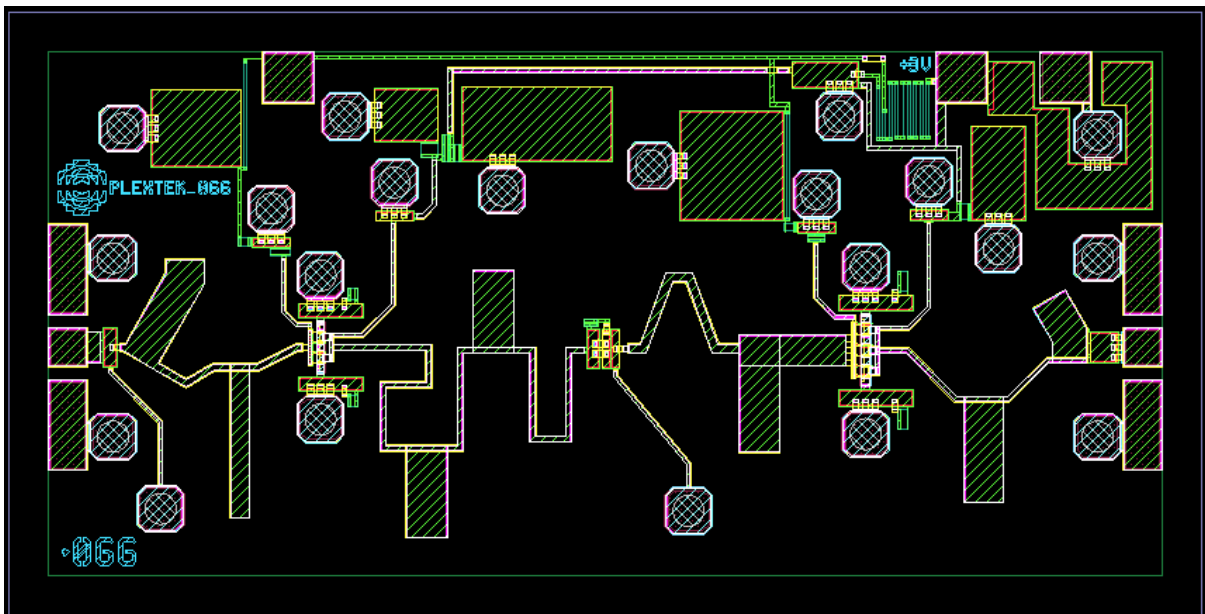
Much of the effort during the design process was devoted to limiting the loss in available gain due to practical implementation details (biasing networks, matching networks and circuitry to ensure stability). A simplified schematic of the biasing network used for each transistor is shown in Figure 4. This also includes components to ensure stability below the operating band where the transistors have a large amount of available gain.

RSB and CSB are the self bias components discussed above. In reality parallel copies of this network are included on each side of the transistor to reduce grounding inductance. Gate and drain bias is injected through transmission lines TL1 and TL2. The remote end of the transmission line (the bias injection point) is grounded through a capacitor CRF. The dimensions of the capacitor were selected to provide a good in-band short-circuit and the lengths of TL1 and TL2 then adjusted to transform this short-circuit to an open circuit at the transistor. At lower frequencies, well below band, the capacitor CRF is not large enough to provide a good short-circuit. This provides an opportunity to introduce stabilizing resistors RGB and RGD, which are connected to ground through capacitors CGB and CGD. These capacitors are much larger than CRF and provide good low impedance paths down to below 1GHz. Off-chip de-coupling can be used to assist with ensuring stability at frequencies below this. Low cost SMT capacitors can be used for this purpose and more expensive microwave Single Layer Capacitors (SLCs) are not required.
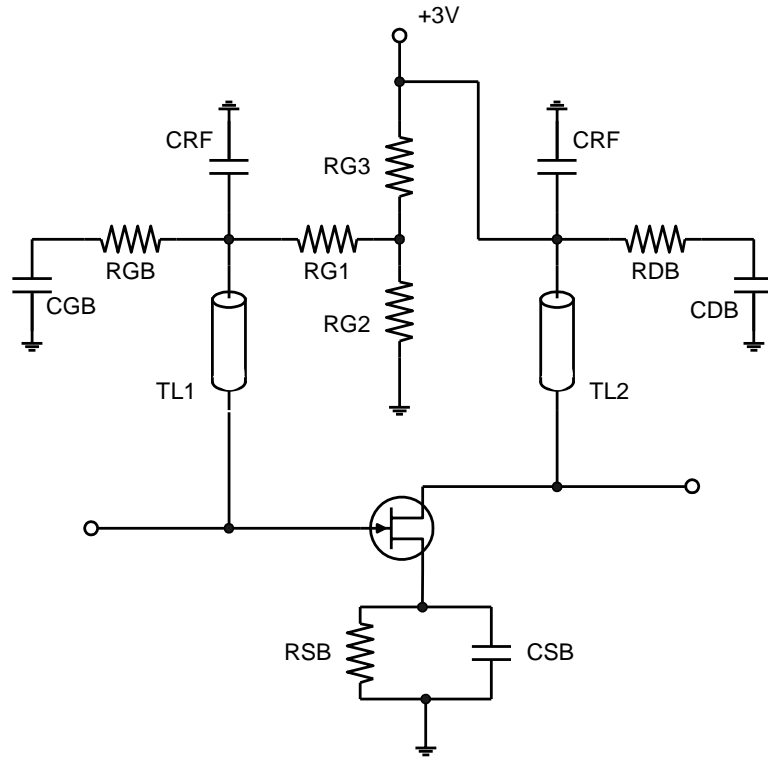
**Figure 4: Simplified schematic of transistor biasing and low frequency stabilising network**

The next step in the design process was to implement matching networks. Low-pass distributed structures comprising narrow series transmission lines and open-circuit stubs were used for this purpose. Short-circuit stubs were also introduced as a means of further improving low frequency stability. Some modest resistive elements were introduced into the gate bias stubs to provide frequency selective loss and flatten the gain versus frequency response. These elements are all evident from inspection of the layout plot in Figure 5.


Figure 5: Layout of the 60GHz driver amplifier

One of the key difficulties throughout the design process was in ensuring the accumulated losses incurred in the practical implementation did not excessively degrade the gain. In the first instance the design was completed based on circuit simulated models (transistors, capacitors, resistors and transmission lines from the Process Design Kit (PDK)). The simulated s-parameters for this case are reproduced in Figure 6. Gain is around 10dB and matches better than 15dB. The amplifier is biased from a single +3V supply (at one pad of the IC) and draws a total current of 36mA.

The next stage in the design process was to EM simulate the metalwork and re-optimise the design to compensate for the discontinuity and proximity effects that became evident. This process was completed step by step with increasing amounts of the circuit gradually EM simulated. Compensation for the EM effects was undertaken as this process progressed. One of the most significant consequences of the EM simulation was to reduce the gain. Careful re-optimisation was undertaken at each stage to try to avoid reducing the amplifier's gain. The simulated s-parameters of the final circuit including EM are plotted in Figure 7. The gain is now reduced to around 9dB but is still flat across the operating band. Input and output return losses are still better than 15dB.
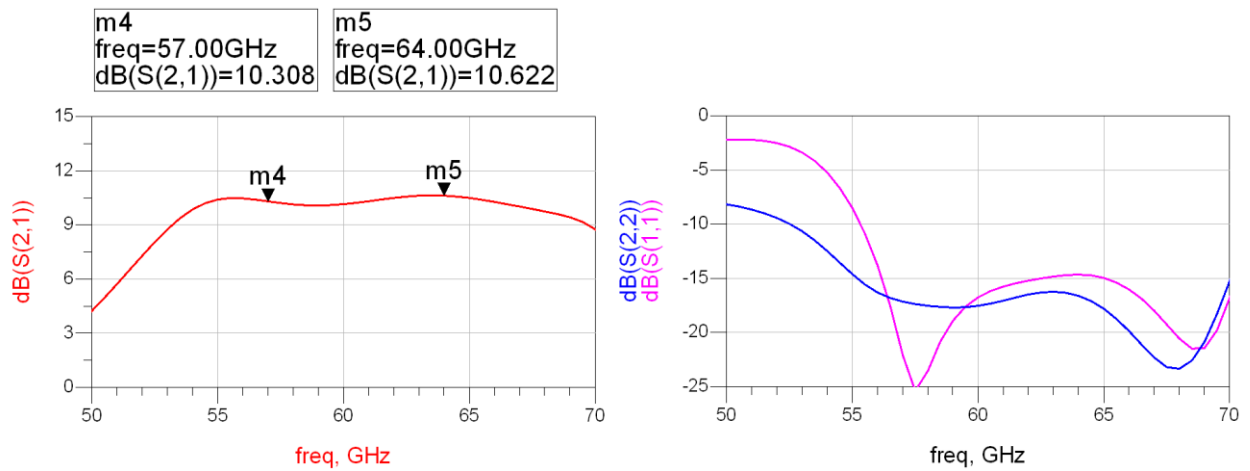
Figure 6: Simulated s-parameters of initial (circuit-simulated) design
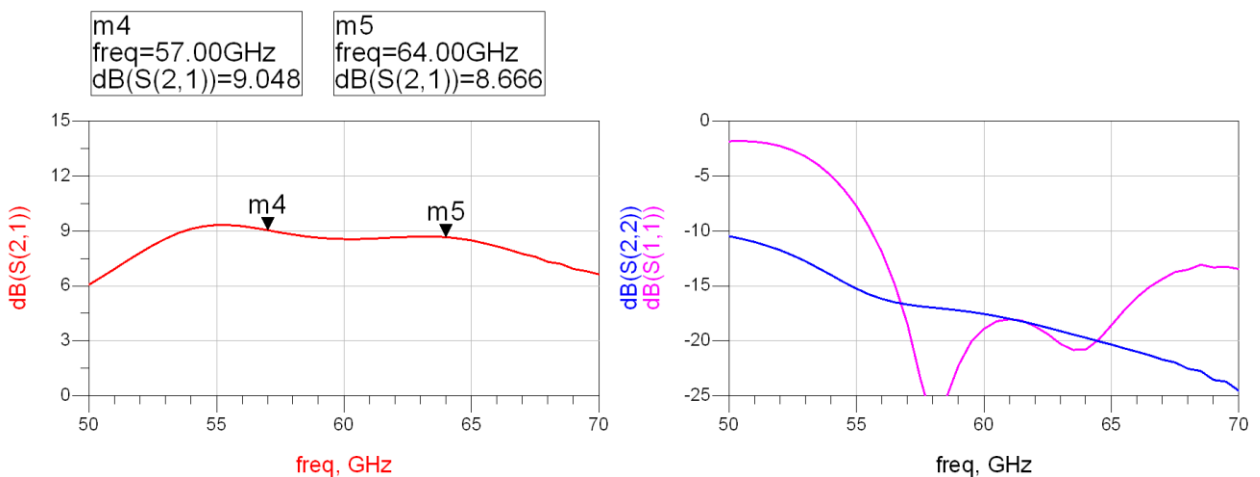
Figure 7: Simulated s-parameters of final design including EM

The simulated P-1dB of the final design, including EM, is plotted against frequency in Figure 8 and is over +13dBm. The stability factor is plotted to 100GHz in Figure 9. It is vital to confirm stability above and below the operating band as well as in the band itself.
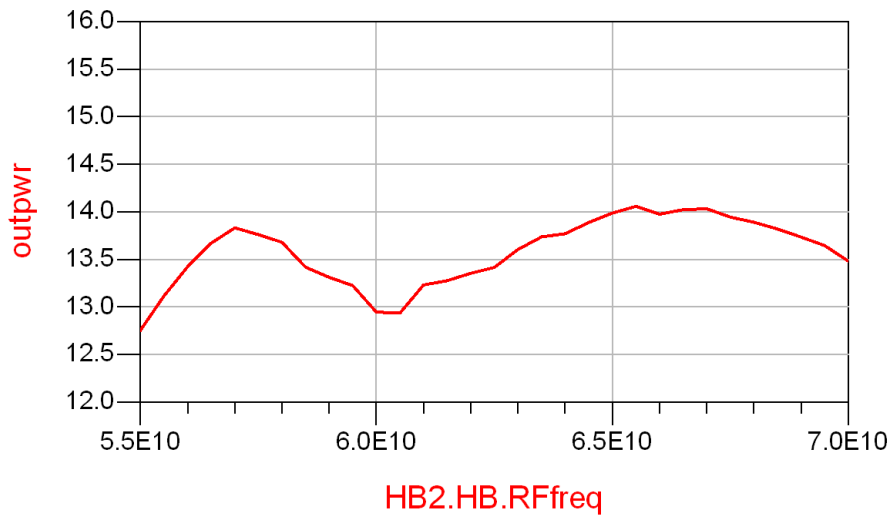
Figure 8: Simulated P-1dB of final design including EM
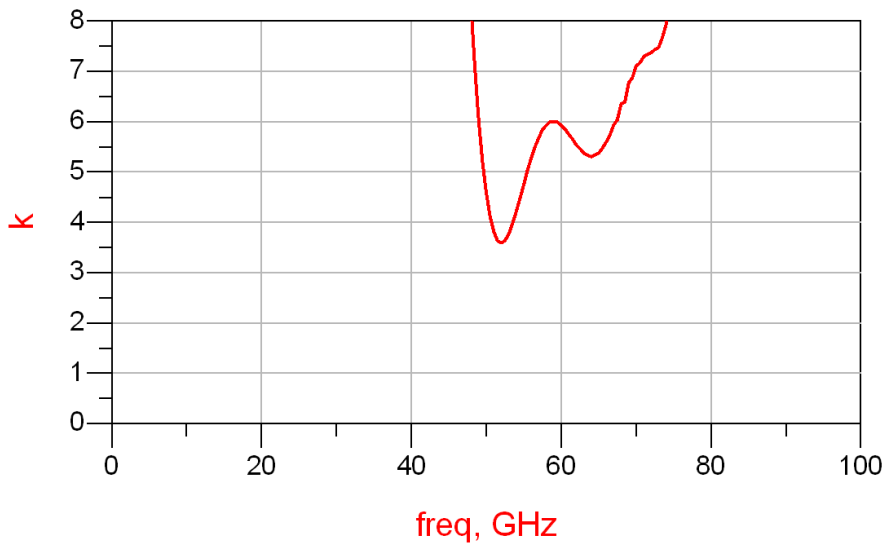

Figure 9: Simulated stability of final design including EM

Fabrication and Measured Performance

At the time of writing the IC has just completed fabrication; a photograph of one of the die is shown in Figure 10. RFOW measurement is scheduled but has not yet taken place.
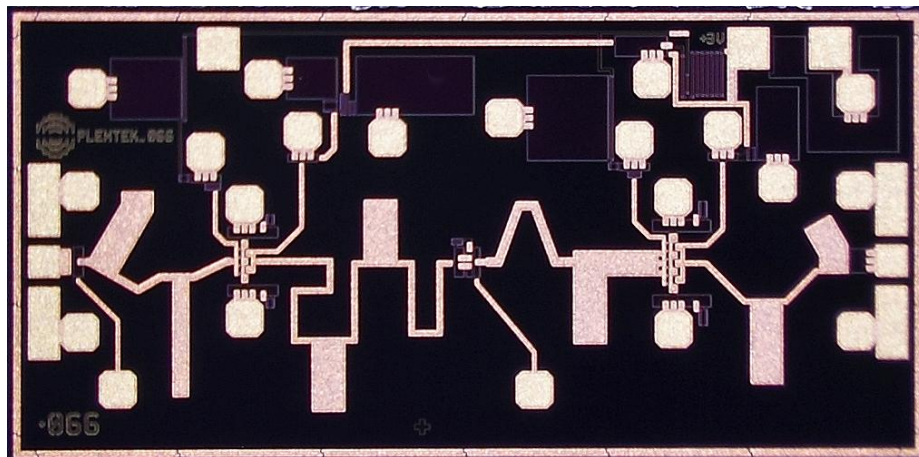

Figure 10: Photograph of the 60GHz amplifier

References

[1] J.A. Wells, "Multi-Gigabit Microwave and Millimeter-Wave Wireless Communications," Boston, Artech House, 2010

[2] Liam Devlin, Stuart Glynn, Graham Pearson, Andy Dearn, "The Design of E-band MMIC Amplifiers", proceedings of the RF and Microwave Society (ARMMS) Conference, April 19th and 10th, 2010