A Monolithic, Dual Channel, 0.5 to 20GHz Limiter

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Abstract - This paper details a dual channel limiter IC, fabricated as a single die using a commercially available PIN diode process. The measured performance shows a small-signal insertion loss of less than 0.8dB from 0.5 to 20GHz with excellent channel matching. The limited output power (at 10dB saturation) measures between 15 and 16.5dBm, across the band. The IC can handle CW power levels of 4W and had an RF yield of 93%.

I. INTRODUCTION

The dual channel limiter IC was designed to provide receiver protection for a broadband monopulse Electronic Support Measures (ESM) antenna system [1]. The antenna system provides eight outputs arranged in monopulse pairs operating from 2 to 18GHz. Each monopulse pair must track accurately both in amplitude and phase so that bearing accuracy is maintained. This tracking was best achieved with a monolithic implementation.

PIN diodes are a popular technology choice for limiter realisations because they are able to handle relatively large amounts of power using a comparatively small device. An integrated realisation allows accurate channel matching and results in low parasitics which facilitates the very large operating bandwidth of the design. Triquint Semiconductor Texas' Vertical PIN diode (VPIN) process was selected for the realisation of the Monolithic Microwave IC (MMIC).

II. PIN DIODES AS LIMITERS

A PIN diode takes its name from its structure; it comprises a region of high resistivity intrinsic material sandwiched between a region of P-type semiconductor and N-type semiconductor. When the PIN diode is forward biased, charge carriers are injected into the I region lowering its resistance. Thus at RF and microwave frequencies a PIN diode behaves as a current controlled resistor. They are optimised to achieve wide resistance range, good linearity, low distortion, low drive current and high power handling capability. These properties mean that PIN diodes can be configured to make excellent RF/microwave switches and also find applications in variable attenuators and phase shifters. Figure 1 shows an equivalent electrical circuit model for a PIN diode at RF/microwave frequencies. A model for a discrete, packaged diode would also need to incorporate appropriate packaging parasitics.

The forward current through the diode controls its resistance, Rj. For zero or reverse bias, with no current flowing, the resistance Rj is high, in the region of several kΩ. As the forward bias current through the diode is increased, the charge carriers injected into the I region reduce the value of Rj to values as low as one or two ohms, depending on the diode structure.

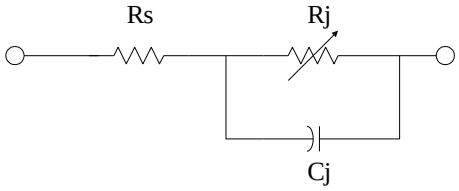


Figure 1: ELECTRICAL EQUIVALENT MODEL OF A PIN DIODE

When configured as a limiter, diodes are normally mounted in shunt to ground. When high power RF signals are present, charge carriers are injected into the I region of the diode on one half cycle and removed on the opposite polarity half cycle. Imperfections in the I region and statistical considerations mean an accumulation of charge develops in the I region reducing the diode's resistance. This charge generation also results in a DC current (a rectified portion of the RF signal) which must have a DC return path in order for the limiter to function properly.

Figure 2 shows the circuit diagram of a limiter from [2]. The RF choke provides the DC

return, which the diodes need to function as a limiter, whilst providing an open circuit at RF to avoid attenuation of the wanted signals.

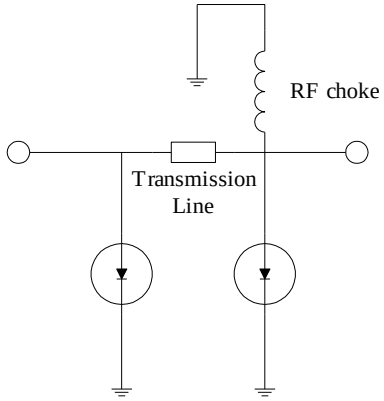


Figure 2: LIMITER CIRCUIT, FROM [2]

An alternative topology which does not require an RF choke is shown in Figure 3 (from [3]).

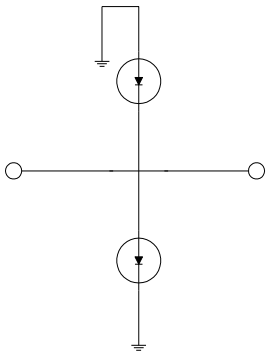


Figure 3: LIMITER CIRCUIT, FROM [3]

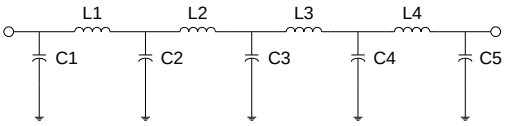
In this case two back to back diodes are used. Charge is injected into the I region of each diode on alternate half cycles and each diode acts as the DC return for the other's rectified current.

III. CIRCUIT DESIGN

PIN diodes fabricated on the Triquint Texas' VPIN process have very low off state capacitance, which makes them suitable for use up to mm-wave frequencies.

The design methodology adopted, to cover the desired 0.5 to 20GHz frequency range, was to absorb the parasitic capacitance of the diodes within a filter structure. This conveniently allows multiple stages of shunt diodes to be incorporated into the design, which provides limiting to slightly lower power levels than with a single diode pair.

The starting point for the design was a 9th order maximally flat (Butterworth) low pass filter [4] with a cut off frequency of 21GHz. A schematic of the filter with component values is shown in Figure 4.



C1	0.053pF	L1	0.379nH
C2	0.244pF	L2	0.712nH
C3	0.303pF	L3	0.712nH
C4	0.244pF	L4	0.379nH
C5	0.053pF		

Figure 4: 9TH ORDER LOW PASS FILTER

The next step was to replace the centre three shunt capacitors by antipodal diode pairs. The reason a 9th order filter was used as the basis for the design, in preference to a lower order filter, is because it results in larger values for the central three shunt capacitors. This means the size of the diodes used to replace them can be larger, which increases the maximum power handling capability of the limiter.

DC blocks were also added to the input and output of the filter and the series inductors were replaced by short lengths of high impedance transmission line. The required values of the series inductors are so small as to make this technique well suited to MMIC realisation but impractical for hybrid assemblies operating across this frequency band.

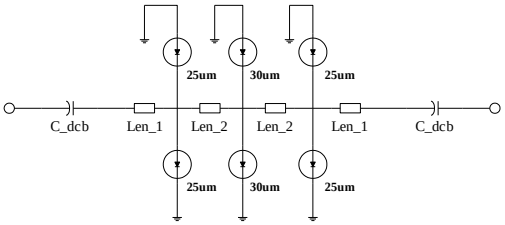


Figure 5: SCHEMATIC OF LIMITER CIRCUIT

The next step was to optimise the values of the series inductive elements and end shunt capacitors to achieve low insertion loss across the operating band. Bonding interface parasitics were also included to ensure optimum performance of the assembled die. The final circuit schematic of one channel of the limiter is shown in Figure 5. Note that the outer two shunt capacitors are omitted as their value tended towards zero in the final stages of the filter optimisation.

Figure 6 shows the final small signal simulated performance of the limiter, including all discontinuity models, DC blocking capacitors and bondwire interface models. Large signal simulations of the circuit were not possible, as suitable models were not available.

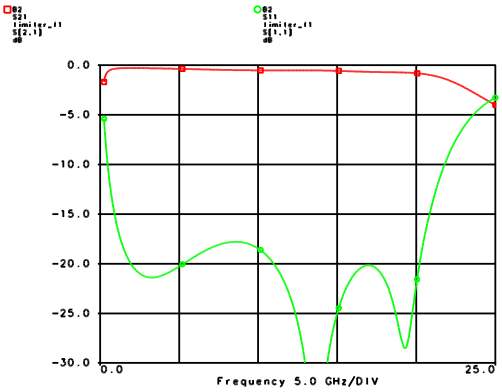


Figure 6: SIMULATED SMALL SIGNAL PERFORMANCE, INCLUDING BONDING PARASITICS

It was intended to perform RF On Wafer (RFOW) measurement of the limiter using a Through Reflect Line (TRL) calibration. This means the RFOW performance of the limiter would be different to that simulated for the assembled die, which included bonding parasitics (Figure 6). The predicted RFOW performance, assuming a TRL calibration, of the limiter is shown in Figure 7.

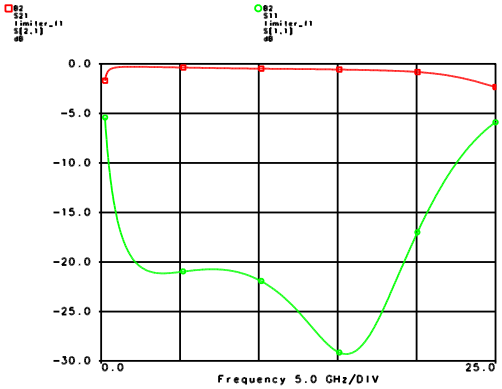


Figure 7: PREDICTED RFOW, SMALL SIGNAL PERFORMANCE (TRL CALIBRATION)

IV. MEASURED PERFORMANCE

A photograph of one of the dual channel limiter die is shown in Figure 8. The size of the die has been increased, beyond the minimum required, to fit in with the arraying of other circuits fabricated on the same mask set. This allowed the TRL calibration structures to be included on the die.

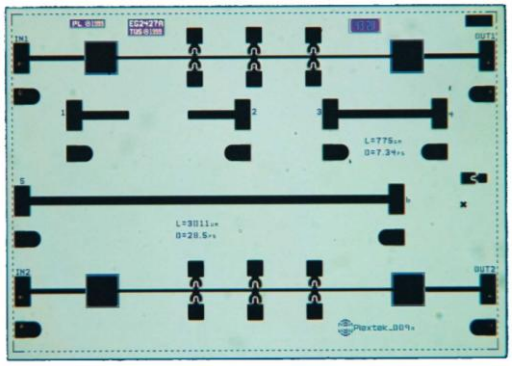


Figure 8: PHOTOGRAPH OF ONE OF THE DUAL CHANNEL LIMITER DIE

The small-signal s-parameters of all limiters, from 4 wafers have been measured. Figure 9 compares the RF On Wafer (RFOW) measured performance against simulated. The measured insertion loss is less than 0.8dB from 0.5 to 20GHz and is in very good agreement with the simulated. The measured return loss is lower than the simulated but is still better than 14dB across most of the band, degrading very slightly at the band edges. The average RF yield was 93%.

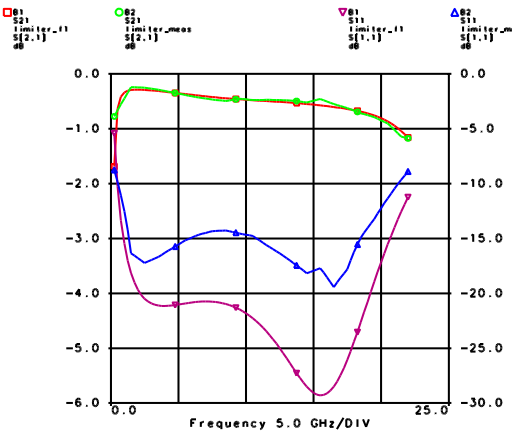


Figure 9: RFOW MEASURED VERSUS SIMULATED SMALL-SIGNAL PERFORMANCE

The power compression (signal limiting) performance was measured on a sample (5%) basis. Test equipment limitations meant that the highest output power, which could be generated at the probe tips was +25dBm. However, when measured the limiters were around 10dB into saturation at this input power level. Figure 10 shows a plot of the power compression characteristics of a typical limiter measured at frequencies of 2, 5, 12 and 18GHz. The limited output power was between 15 and 16.5dBm.

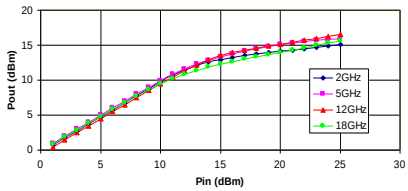


Figure 10: OUTPUT POWER VERSUS FREQUENCY, INPUT POWER IS 0 TO +25dBm

The amplitude and phase matching between channels is an important parameter in the ESM application for which the limiters were designed. As might be expected, the channel matching is excellent, within 0.1dB and 1°.

Limiter die were subsequently assembled into dual channel modules for evaluation in the monopulse ESM system. Figure 11 shows a photograph of one of the modules. Power transfer measurements have been carried out to much higher power levels than were possible on wafer. Figure 12 shows the measured power transfer characteristics of a limiter module at 10GHz. The peak output power level is +17.9dBm.

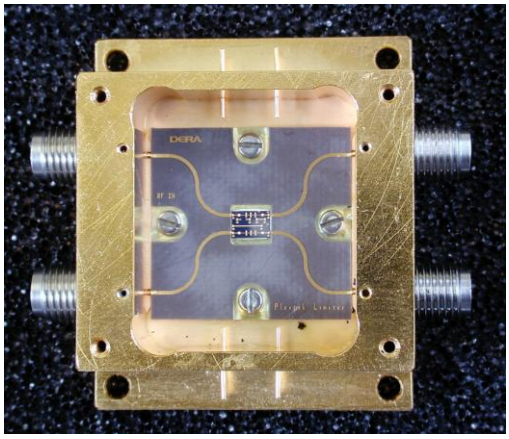


Figure 11: PHOTOGRAPH OF A DUAL CHANNEL LIMITER MODULE

The "kink" in the characteristics of Figure 12, at around +30dBm input, is a real and repeatable feature. At power levels below this, most of the limiting is due to the first pair of diodes. Insufficient power is getting past them to cause the subsequent diodes to move significantly into forward conduction. At input powers beyond 30dBm, the second pair of diodes also start to turn on and provide additional attenuation.

A number of limiters have been tested to destruction. The input power level, which was required to cause destruction, was around +39dBm at 5GHz and around +37.5dBm at 17GHz. After destruction, the limiter continued to provide protection but the small signal insertion loss had increased to a level which would necessitate replacement of the module for continued operation of the system.

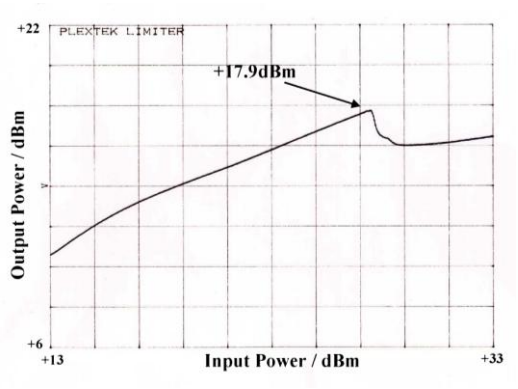


Figure 12: POWER TRANSFER OF LIMITER MODULE AT 10GHz

V. CONCLUSIONS

A monolithic dual channel limiter IC has been designed, fabricated and measured. It has very low small signal insertion loss (< 0.8dB) from 0.5 to 20GHz and an average RF yield of 93%. The saturated output power (at 10dB compression) of the limiter is between 15 and 16.5dBm across the entire band and it can handle CW power levels of 4W. Amplitude and phase match between the channels is within 0.1dB and 1°.

VI. ACKNOWLEDGEMENTS

The authors would like to thank Jim Carroll and Lisa Howard of Triquint Semiconductor Texas for their help during this development.

VII. REFERENCES

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