A Universal GaAs HBT PA with Active Bias Circuitry, Covering 4.9-6 GHz

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***Abstract* — This paper describes the design, fabrication and measured performance of a 4.9 to 6GHz Power Amplifier IC developed on a commercially available InGaP HBT process. It can address a number of applications including U-NII (US FCC), 802.11a, HiperLAN2, Japanese WLAN and cordless telephony. The amplifier was designed to operate from a 3.3V supply in either linear mode (backed off several dB from gain compression) or saturated mode (at an output power level of 0.5W). The quiescent current is kept low by an active bias circuit, and rises with increased input power to yield optimum efficiency in all modes. The active bias circuit also serves to extend the region of linear gain by appropriate dynamic control of the transistor's base voltages. The amplifier requires a simple off-chip output matching network that can be tailored to satisfy a customer's exact frequency/power requirements.**

I. INTRODUCTION

Indium Gallium Phosphide (InGaP) HBT processes are well suited to the realisation of efficient, high linearity, RF and microwave power amplifiers. This paper describes a two stage design covering 4.9 to 6GHz, which was designed by Plextek Ltd. and realised on the commercially available InGaP Power HBT process of GCS Inc. This process has a Ft of 45GHz, a Fmax of 55GHz, and is capable of generating 2.5W of output power per cm^2 of active device periphery.

II. MMIC DESIGN

The circuit is a two-stage class AB design that uses a novel, current-mirror based, active bias circuit to optimise bias current with drive level and to extend the linear gain region of the amplifier. The general schematic for the amplifier is shown in Fig. 1, and a photograph of the fabricated MMIC is shown in Fig. 2.

The first stage uses series resistive feedback and has an on-chip input matching network. The second stage is a large HBT device (consisting of 40 x 42μm^2 emitter fingers), with a collector-coupled output. Inter-stage matching is included on-chip between the two stages. +3.3V is applied directly to the collectors of each stage via on-chip choke and de-coupling networks. Different configurations of active bias circuit are used to control the base currents of the two stages, with each also being designed to improve linearity when the amplifier is operated backed-off from compression.

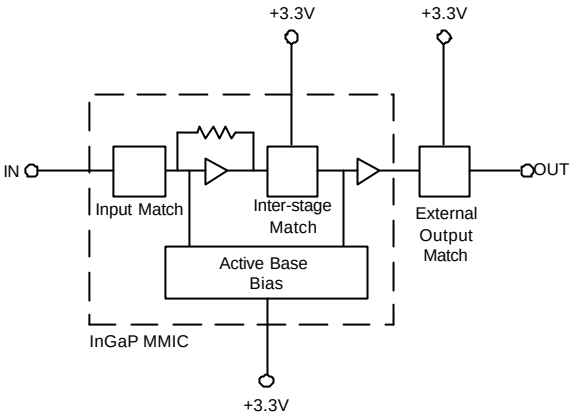

Fig. 1: Amplifier Schematic

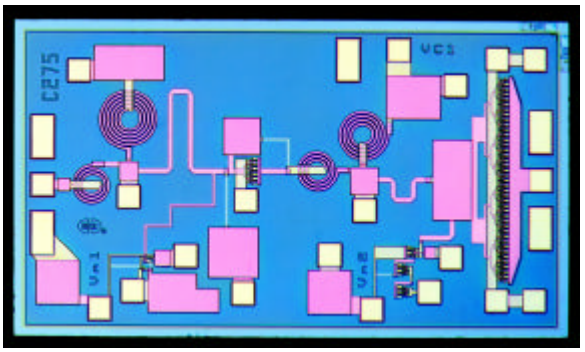

Fig. 2: Amplifier Photograph

The active bias circuit to the first stage amplifier is shown in Fig. 3. The circuit utilises a simple current mirror technique [1] but with a capacitor added to improve the linearity of the gain [2], and an RC filter to stop RF leakage through the bias circuitry. The active bias to the second stage is similar, except that stacked diodes are used to set the reference voltage to the current mirror device. This time the RC filter is not necessary, but again a capacitor is used to improve linearity.

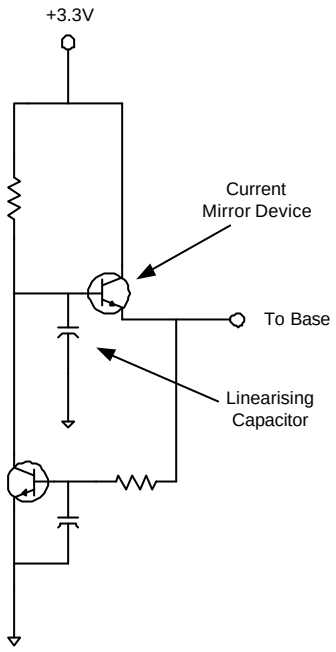

Fig. 3: First-stage Active Bias Circuit

The effect of optimising the two linearising capacitors is best illustrated in Fig. 4. These graphs illustrate the magnitude (in dB) and phase (in degrees) of the gain of the output stage, biased through its active bias circuit, with and without the linearising capacitors. Without the capacitors both the Magnitude and phase of the gain are highly non-linear with respect to the input power drive level, well before saturation occurs. With the capacitors, linearity holds right up until the device begins to saturate.

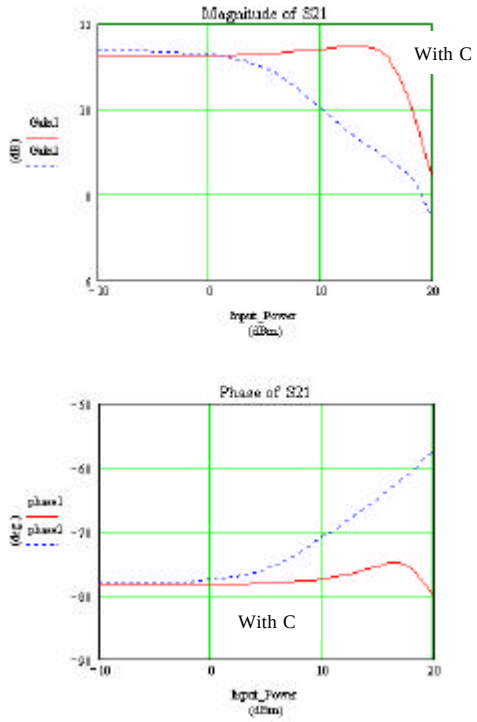

Fig. 4: Effect of Using Linearising Capacitors on Output Stage Gain

III. MEASURED PERFORMANCE

The performance of the IC was measured when mounted on a test PCB. The test circuit was manufactured on 0.020" thick Rogers RO4003 material. The MMIC was attached with silver loaded epoxy, and the input, output and bias connections formed by gold wire bonding. As with most high power, high performance RF PAs, the output is collector coupled and requires a simple off-chip matching/biasing network. A simple shunt-C, series-L, shunt-C matching configuration was used to cover the entire 4.9 to 6GHz band. The capacitors were 0402 outline, and the inductor was realised as a printed track on the PCB. Fig. 5 shows the small-signal measured gain and output match.

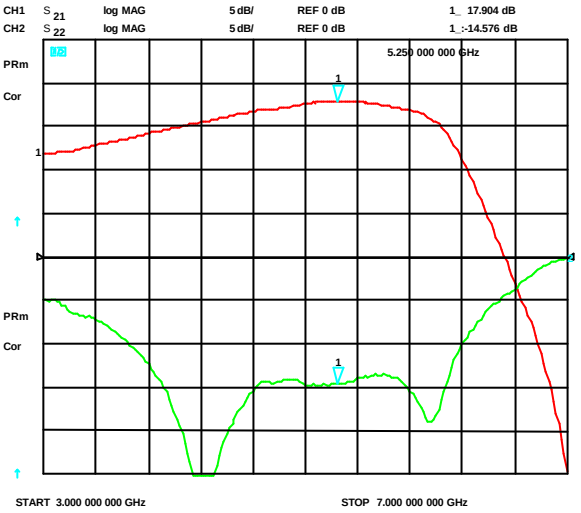

Fig. 5: Small-signal S-parameter Measurement

Gain is just below 18dB at 5.25GHz, falling to just less than 17dB at 5.85GHz. The output return loss is better than 13dB across the 4.9 to 6GHz band, and the on-chip matched input also has a return loss greater than 10dB.

The measured power transfer characteristics (at 5.25 GHz) are illustrated in Fig. 6. It can be clearly seen that when the amplifier is used backed off by approximately 8dB from 1dB compression that:

- The gain is very flat
- The current drain is much less than that at power compression

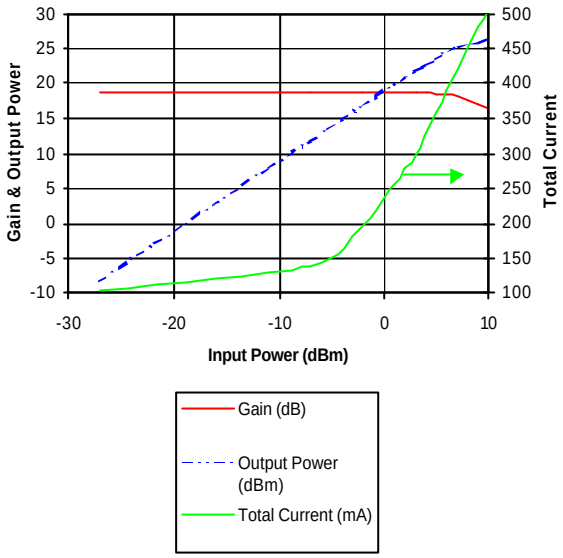

Fig. 6: Large-signal Measurement

It can also be seen that the active bias network assists in dynamically adjusting the amplifier's bias with input power level to obtain a flat gain versus power characteristic and avoiding a soft compression characteristic. This optimises the linearity of the amplifier. At small input signal levels the quiescent current is low at 100mA, and this grows with increasing input power to 212mA at +18dBm linear output power, and to around 400mA when used at 1dB power compression (+25.7 dBm output power).

The output referred third order intercept point (OIP3) of the amplifier is also greatly improved by the linearisation technique. Fig. 7 shows the resulting third order intermod products measured using two input tones separated by 10 MHz, to give a total output power of +18dBm (+15dBm per tone). The measured OIP3 point is +37.5dBm.

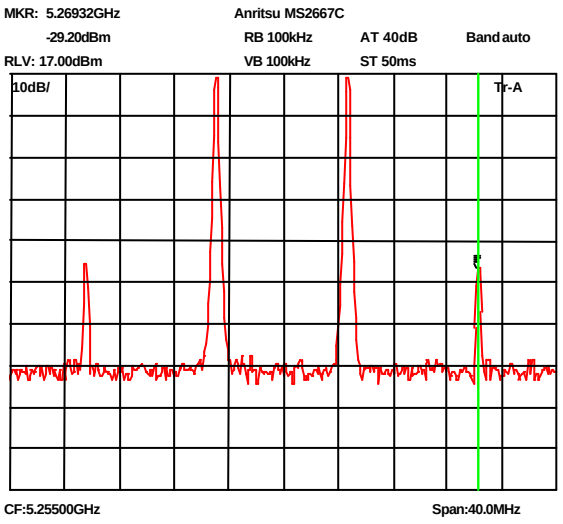

Fig. 7: Third Order Intermods Measurement

A summary of the amplifier's measured performance is given in Table 1. Results at 5.8GHz are very similar to those at 5.2GHz. All of the reported measurements use the same external output matching circuit, optimised for wideband (4.9 – 6GHz) operation. In practice, the output match could be tailored to specific narrow bands to further improve the RF performance.

Parameter	***Measurement @ 5.25GHz***	***Measurement @ 5.85GHz***
Gain	17.9 dB	16.7 dB
Input Match	-16 dB	-15 dB
Output Match	-14.5 dB	-16.5 dB
Total Quiescent Current	100 mA	102 mA
Total Current at +18dBm linear output	212 mA	210 mA
Output Power at 1dB compression	+25.7 dBm	+23.7 dBm
Total Current at 1dB compression	402 mA	385 mA

Table 1: Summary of Broadband Matched PA Measurements

IV. CONCLUSIONS

This paper has presented the design, realisation and measured performance of a 4.9 to 6GHz InGaP HBT power amplifier MMIC designed on a commercially available InGaP HBT process. It can be used for a range of applications including U-NII and 802.11a. It incorporates an on-chip active bias arrangement that is optimised to dynamically control the amplifier bias to realise low quiescent current drain, high linearity when backed-off from compression (at output power levels of up to +18 dBm), and good efficiency when operated with 0.5W saturated output power. The amplifier draws low quiescent current of 100mA at low output powers, rising to 212mA at +18dBm output power, and 400mA at 1dB power compression (+25.7 dBm output power).

REFERENCES

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