RF ICs FOR COMMERCIAL WIRELESS APPLICATIONS

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Introduction

Prior to the advent of the commercial wireless communications market in the late 1980's, most RF circuit designs were destined for military applications. Since then, the size of the military market has declined, whilst the size of the wireless communications market has grown exponentially. With the move from low volume military applications to high volume commercial applications came ever increasing pressure for reduced cost, size and weight. This paper discusses the important trade-offs which must be made when designing RF ICs for use in high volume commercial wireless products and presents techniques which can be adopted to keep the costs down to the very low levels demanded by the market.

Comparing Integrated RF Circuits With Discrete

Integration provides a means of significantly reducing the size and weight of a product. The total number of components used in the product is also reduced, which will improve assembly yield. If the volumes are sufficient, it is also possible to achieve significant BOM cost savings through integration. Since portable wireless communications product designers are continually striving to reduce the size, cost and weight of their products, the use of integrated circuits would clearly seem appropriate.

In virtually all of the portable wireless communications products available today, the vast majority of the IF and baseband circuitry is integrated. However, in many cases discrete components are still used extensively throughout the RF section. Given the advantages outlined above, this may seem short sighted but when it comes to designing RF circuits, a discrete realisation still has much to offer [1]. Although an integrated design will offer reduced size, weight and component count, a discrete realisation has a number of important advantages: A mix of technologies can be used throughout the design. Perhaps an inexpensive PIN diode T/R switch followed by a discrete bipolar LNA and a high linearity diode mixer. With an integrated design the device type(s) of the chosen technology must be used throughout.

Other benefits of performing a discrete design, are increased speed of implementation, ease of modification and significant reductions in development costs. This said, if a product designer has a suitable integrated circuit available at the outset, then the development time and effort required for the whole product design can actually be reduced by the use of ICs [2]. Whilst the use of ICs can undoubtedly offer the smallest implementation, significant advances have been made in reducing the package size of discrete components, which has also helped with the continuing size reduction of the end product.

Another advantage of integration is that although the IC designer is restricted to using devices available on the chosen technology, additional devices can be included at a virtually negligible cost increment. These transistors will be virtually identical to other transistors nearby, which allows differential circuitry and active biasing techniques to be exploited. An example of a circuit which makes use of this device similarity is the "Gilbert cell" balanced mixer [3]. It is used almost exclusively in bipolar RF mixer designs and is virtually impossible to realise in a discrete form.

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A summary table comparing the main parameters of a discrete implementation to an integrated is given in Table 1, below.

Parameter	Discrete	Integrated
Development cost	Moderate	Very High
Modifications	Relatively easy and inexpensive	Expensive, generally one or more new masks
BOM cost	Low	Depends on volume, die size and process used
Mixing technologies	Optimum device technology can be used throughout	Limited scope
Parts count	High	Low to very low
Size	Small to medium	Smallest
Weight	Light	Lightest
Cost of using additional transistors	Moderate	Low
Matched transistors	Difficult to use effectively	Very good, used extensively

Table 1: Comparison of integrated to discrete RF circuits

The summary table above suggests that the relative benefits of integrated and discrete implementations are quite evenly matched. However, the use of RFICs in commercial wireless products is increasing. There are 3 reasons why this is happening:

- An increasing number of RF ICs, offering acceptable performance at a competitive price, are now becoming commercially available.
- Product design times can be shortened if suitable integrated circuits are available, since discrete versions need not be developed.
- The use of ICs allows reduced size and weight.

Figure 1 shows a comparison of the sizes of first generation analogue cellular handsets and modern second generation digital cellular handsets. The continuing drive towards smaller handsets is clearly evident.

Figure 1: Size comparison of an early first generation cellular handset to today's (1997) leading edge second generation designs

Level of Integration

When choosing to integrate an RF circuit, decisions must be made as to what level of functionality should be integrated onto a single die. Whilst the highest possible level of integration may offer the largest reductions in size, weight and component count, it may not offer the best technical or commercial solution. Problems may occur because of on-chip cross-talk or the effects of packaging parasitics may unacceptably degrade the

rejection provided by external filters. The consequences of integrating different circuit functions very close together on the same die must be considered.

The versatility of the resulting IC must also be considered. A simple LNA and mixer can find applications in various wireless products, where as a complete GSM transceiver IC is a true Application Specific Integrated Circuit (ASIC) which is unlikely to be used in non GSM products. Consequently it may be decided to partition the functionality of the RF transceiver into a number of ICs. In addition to making each individual IC more versatile, this allows different processes to be used for different parts of the circuit. Whilst a MESFET process may offer good performance for the LNA and mixer, it is unlikely to be the best process for realising the synthesiser.

Another factor which must be considered is die size. A wafer of ICs will cost the same to fabricate whether it contains 10 000 circuits or 100 circuits. Clearly the larger the area the circuit occupies, the more expensive the die. This is compounded by the fact that larger die will also exhibit lower yields. Figure 2 is a graph showing the number of die available from a single wafer versus die size. Wafer diameters of 3", 4" and 6" are considered. The figures take account of the area lost to circuits at the edge of the wafer and make an allowance for area devoted to Process Control Monitor (PCM) cells. Functional yield is not considered since this is a complex function of process defect density, device variation, circuit design and performance specification. However it is certain that yield will degrade with increasing die size.

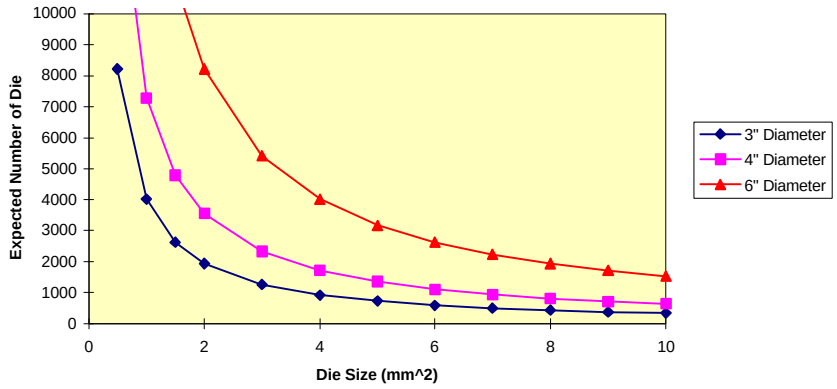

Figure 2: Expected number of die from a single wafer versus die size, for various diameters of wafer

It is not possible to deduce an absolute unit cost versus die size since this will vary from process to process and will also depend on the RF yield achieved and the volumes in which the circuit is being manufactured. However, Figure 2 clearly shows the way in which chip cost is dramatically reduced as the die size falls. It is therefore vitally important, before deciding to integrate a particular circuit function, to evaluate the resulting increase in die size and therefore cost. This cost increase must then be compared to the benefits of having the particular circuit function integrated. For example, integrated passive matching or biasing components for an IF amplifier would occupy a comparatively large die area and would not be cost effective.

Figure 3 is a generic block diagram of a digital wireless transceiver, showing the cost breakdown, in US $, of each sub-circuit. These costs are approximate and reflect high volume (more than 1 million parts per year) pricing. All costs are for discrete implementations, with the exception of the I-Q modulators and the synthesisers, for which integrated realisations are significantly more practical and cost effective and are always used in modern designs.

The filters contained in the block diagram of Figure 3 account for over 40% of the total BOM cost. This is a great pity for IC manufacturers since it is the one part of the transceiver which is virtually impossible to integrate. Even if die area was not important, integrated passive elements [4] of a high enough Q to realise the required filter performance are not practical. Active filter realisations [5] suffer from high noise figure, poor linearity and a high degree of variation both with temperature and from unit to unit. Image reject mixers provide rejection of image noise but filters are still required to reject interfering signals. As the frequency spectrum becomes more congested, future standards are likely to require even more filtering, in an attempt to cram in as many users as possible.

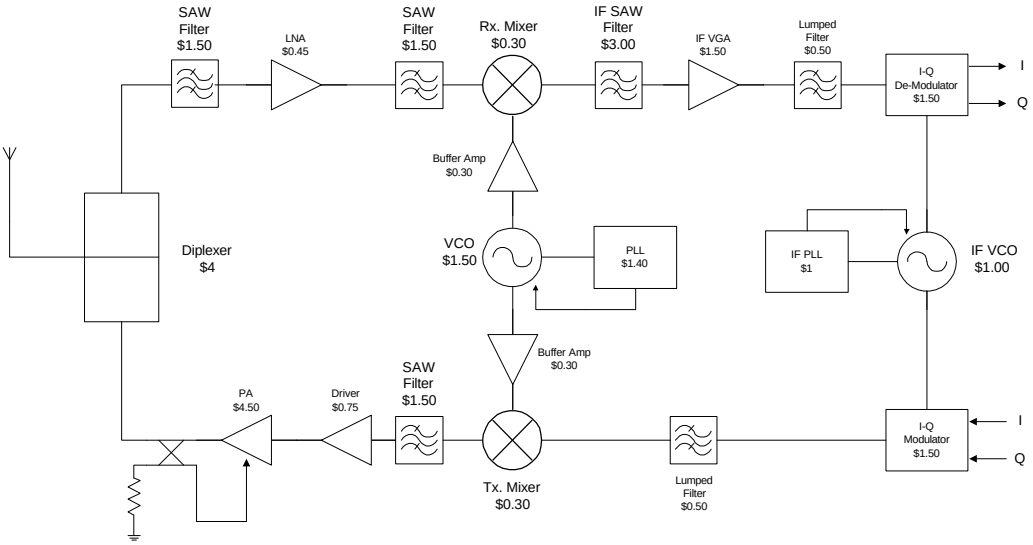

Figure 3: Generic block diagram of a wireless transceiver

The Power Amplifier (PA) is also an expensive item and is a candidate for integration. Although some manufacturers still choose to go to the effort of carrying out a discrete design, many use PA modules which are widely available. Packaged integrated PAs are also available but are normally integrated separately from the rest of the transceiver, since special high power processes are generally used and great care must be taken with the thermal considerations of the package design. Considerations regarding the maximum die size and the most appropriate partitioning of functionality also suggest a separate PA to be advisable.

Other than the PA and the filters, it is possible to integrate any subset of the other functions shown onto a single die. However, it is important to keep in mind the achievable performance and the cost of a discrete realisation. If an IC containing an LNA, a mixer and an LO buffer amplifier is fabricated, then this replaces just $1.05 of discrete parts and this is the price target it must meet. Although there will also be a saving in board area and component count, history has shown that manufacturers are unwilling to look at the advantages offered by RF ICs until their cost can match a discrete implementation [1].

Active Biasing

Discrete RF circuits normally utilise inductors and/or resistors to inject the drain/collector bias and resistors to inject the gate/base bias. Whilst simple control loops are sometimes used to set the bias current, additional active devices mean additional cost and generally the number of transistors used is kept as low as possible. With ICs, additional active devices can be used with minimal cost implications. Indeed, passive components normally occupy more die area than active, particularly at lower frequencies. This results in active biasing techniques being used on a much wider basis.

Figure 4 shows a simple active biasing arrangement which may be employed in a MESFET based process. Q1 is a current sink (although it is often referred to as a current source) operating at Idss and it “sets” the current through the “RF” transistor, Q2. By setting the width of Q1 to a fraction of the width of Q2, the Ids of Q2 is set to a prescribed percentage of the Idss. The similarity of close proximity devices ensures that this is true across the wafer and from batch to batch. Q3 is an active load, with a high RF impedance but a low DC impedance. It has a fixed gate voltage and acts as a source follower with the source settling at the value required to supply the current dictated by the constant current sink Q1.

The gate and drain of Q3 are RF coupled using a capacitor. This capacitor need only be large enough to have a small reactance, at the frequency of interest, compared to the value of the biasing resistors R1 and R2. Without this capacitor present, R1 and R2 act as a potential divider across the gate of Q3 which results in RF

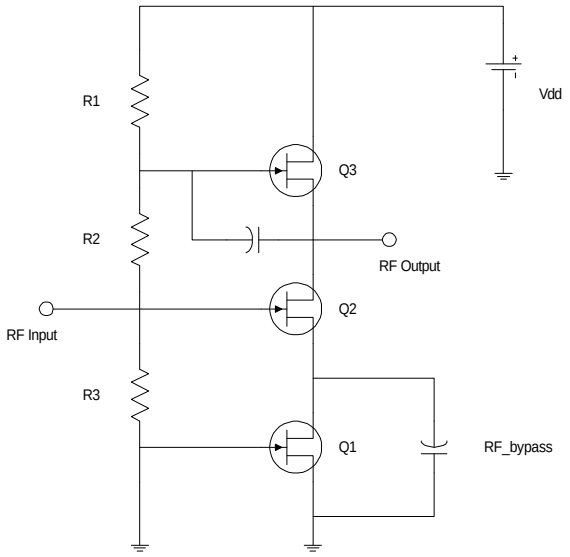

Figure 4: Simple MESFET active biasing arrangement

modulation of the current through Q3. At higher RF frequencies, the Cgs of the transistor will become a low reactance compared to the value of the biasing resistors and this problem will no longer be evident.

A bypass capacitor is required across Q1, to provide a good RF ground. However this is not necessary if a differential amplifier is required, when the high impedance of Q1 will provide improved common mode rejection.

Over the years some very accurate and sophisticated IC biasing techniques have been developed. More details can be found in [6].

Decoupling

Another aspect of discrete transistor biasing is the use of comparatively large values of de-coupling capacitors to provide good RF grounds. In contrast, integrated de-coupling capacitors are much smaller because large capacitors occupy a large chip area which increases die cost. This can lead to problems with low frequency stability, since the decoupling capacitors do not represent a low impedance path to ground. Additional off-chip discrete capacitors can be specified but it also sensible to use resistive de-coupling, when possible. Even a few ohms of resistance in series with the drain/collector supply can make a significant difference to the stability and sensitivity to bias port impedance.

Particular care should be taken when linking drain/collector bias lines on chip (or at a common package lead). This will provide an external feedback path which can result in stability problems. Once this internal feedback path is provided, there is little which can be done externally to rectify the situation.Figure 5 shows the simulated performance of a two stage amplifier designed on GMMT's F20 process and Figure 6 shows the low frequency stability problems which occur when the drain bias points of each stage are directly linked.

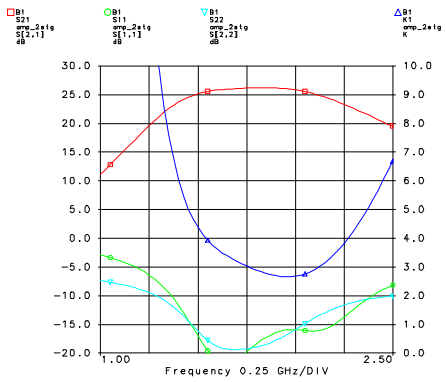

Figure 5: Two stage amplifier, separate drain supplies

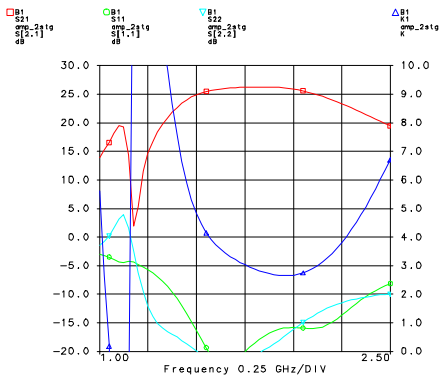

Figure 6: Two stage amplifier, linked drain supplies

When the drain supplies are linked, the output reflection coefficient becomes positive at around 1.1GHz and the stability factor drops well below unity. Both of these factors are indicative of serious stability problems and it is likely that if configured like this, the amplifier would oscillate. Figure 7 shows how this problem can be avoided with the inclusion of a 5Ω resistor in series with the drain bias line of each stage.

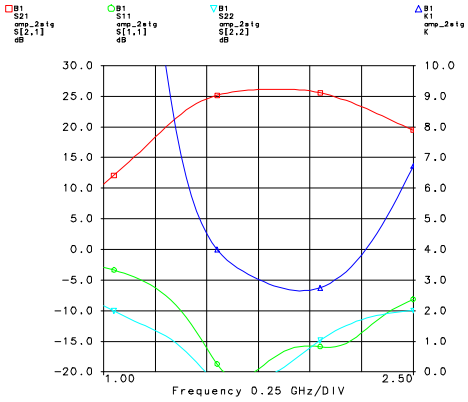

Figure 7: Two stage amplifier, linked drain supplies with resistive de-coupling

Crosstalk

Crosstalk refers to the interference of a signal due to the unwanted coupling of energy from a different signal. It is reduced by shielding, de-coupling and physical separation. If two different signals are simultaneously present on the same die, there will be crosstalk. A classic example of this is found in the disastrous consequences of attempting to use a dual synthesiser IC with different comparison frequencies. Cross talk between the charge pumps operating at the different frequencies can give rise to "glitches" at frequencies which are too low to be suppressed by the loop filter. It is not possible to provide shielding, separation or adequate de-coupling between the two synthesiser loops to solve this problem. Figure 8 shows the output spectrum of a synthesiser where this problem has occurred. The difference between the two comparison frequencies, which were used, was 25kHz and this has given rise to spurious products at 25kHz spacing. If two single synthesiser ICs had been used instead, then this problem would still occur but it would be possible to address it.

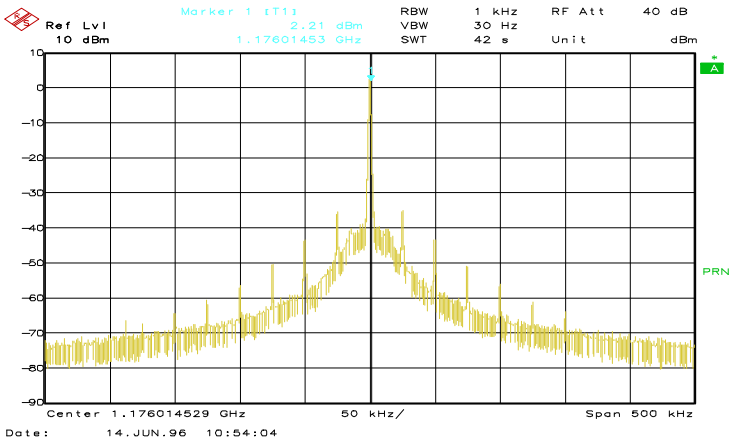

Figure 8: Crosstalk causing 25kHz spurious products in a dual synth. IC

The unavoidable close proximity of circuits fabricated on the same die mean that cross-talk will always occur whenever multiple signals are simultaneously present. Reducing the level of cross talk once the die have been fabricated is not practical. It is therefore not recommended to fabricate circuits which require full duplex operation, such as transceivers for IS-95 CDMA handsets, as single die.

Differential Circuitry

Differential signals have traditionally been used as a means of allowing the amplification of very small signals. The signal can be considered as the difference between two signals in anti-phase to each other. A benefit that differential, or balanced, signals have for use in RF ICs is that they are not referenced to the PCB ground and do not require low inductance RF grounds. Differential circuits have "virtual earth" points, where the

differential voltages cancel and DC bias and ground return points can be conveniently connected at these points. The ground return paths should have a low DC impedance but a high RF impedance. Single-ended, or common mode, signals are referenced to the PCB ground and will be rejected by the differential circuitry. The higher the RF impedance of the ground return, the better the common mode rejection.

In summary, the use of differential circuitry offers the following advantages:

- Immunity to common lead inductance problems
- DC bias can be injected at "virtual earth" points without the need for low impedance RF grounds
- Rejection of interfering common mode signals

The draw backs to using differential circuitry are the increased chip area required for the additional active devices and matching components and the possibility of users being reluctant to provide a differential interface. However, the increased area argument must be countered by the fact that area savings can be made by virtue of the reduction in the number of RF grounding capacitors which are required. One further draw back is that in some cases, particularly at higher frequencies, differential circuits can require more current to provide the same gain and linearity. This is dependant on the particular IC process being used.

On Chip VCOs

RF ICs have been fabricated which incorporate the entire VCO, including an on-chip resonator and the tuning varactors [7, 8]. However the low Q of the resonators and varactor result in phase noise performance which is not adequate for many modern digital modulation schemes. Integrated VCOs with off-chip varactors and resonators have been used successfully [9], however on-chip VCOs generally tend to suffer from the following problems:

- LO current flowing in the common lead inductance increases LO leakage
- LO frequency is sensitive to pulling as other circuits on the die are switched
- Wide production spread of frequency

The LO leakage problem can be reduced by the using a fully differential oscillator. This will mean the resonator does not require a contact to the PCB ground, which means that much less common mode LO current will flow through the common lead inductance. The problem of production spread of LO frequency is eased if a high tolerance, high Q external resonator is used. Using a separately regulated supply will reduce frequency pulling, as will providing some physical separation on the chip, between the VCO and other circuitry. However, the frequency of integrated oscillators will always be pulled as the other circuitry on the same die is switched and once the die has been fabricated, it is a difficult parameter to reduce.

If an external resonator and varactor are required, there is little of the actual integrated oscillator remaining. Given the potential problems with on-chip VCOs and the limited savings in discrete components they sometimes offer, careful consideration should be given before deciding to integrate them. If they are integrated, care should be taken to make sure they can be used as LO buffer amplifiers if their performance subsequently proves inadequate.

Through Substrate Vias

Many GaAs based processes offer the facility of fabricating though substrate via holes. These offer a means of realising low inductance connections to the back of the die, which is normally the ground. This facility greatly

eases the design process. Without it, all points which must be RF grounded need to be taken to pads at the edge of the die and bonded to ground. Despite the benefits of though substrate vias, designers of ICs for commercial wireless applications should avoid using them as it is an additional process step and is normally one of the most time consuming and costly to perform.

Packaging

The majority of RF ICs used in commercial wireless applications, are packaged in low cost plastic packages which are compatible with high volume surface mount assembly processes. However, the packaging of RF components can seriously degrade the performance and the effects of the package must be considered as an integral part of the design from the outset. The main packaging effects which should be considered are:

- Series inductance to the RF input/output ports
- Common lead inductance between the RF ground of the die and the PCB
- Coupling between package legs
- Dielectric loading as a result of the plastic covering the die
- Loss loading as a result of the plastic covering the die
- Increase in junction to ambient thermal impedance

The effects of loss loading increase with frequency. The losses depend on the type of plastic but are generally relatively low upto about 2.5GHz and increase rapidly above this. Two techniques can be adopted to relieve the problem, air filled plastic packages or conformal coating of the die with a protective low loss dielectric such as polyimide. Using the conformal coating approach allows the standard packaging procedure to be adopted. The air filled packages can yield better performance but require a specialised packaging procedure. It is also worth noting that plastic packages are non-hermetic and can absorb moisture over a period of time which can further degrade the performance. Both die coating and air filled packages also help alleviate this problem.

The effects of dielectric loading are also frequency dependant. In general, broader band designs tend to be quite tolerant but components which are very sensitive to frequency off-sets, such as on-chip VCO resonators, can be seriously effected. The series inductive effects of package leads and bondwires can normally be accounted for with little performance sacrifice at frequencies up to several GHz. The coupling between pins can also be accounted for, with sensible layout choices such as making pins requiring isolation non-adjacent. Perhaps the most debilitating parasitic to effect the RF performance of a packaged die is the common lead inductance. This is discussed in more detail below, however, like all of the packaging parasitics described above, it's effects can be accurately predicted if a good electrically equivalent package model is used. The complexity of a package model depends upon the frequency of operation up to which it must be accurate. Reference [10] describes the development of a specific package model.

Whilst accurate package models are necessary to precisely determine the ultimate packaged performance, it is important to have a good understanding of the sorts of problems package parasitics can cause. A packaging effect which is often overlooked and can cause serious performance degradation, is common lead inductance. This is the inductance between the die ground (normally the die attach area) and the PCB ground. It is the parallel combination of the inductance of all package legs (and bondwires) connecting the die attach area to the PCB ground. Figure 9 is an example of a typical bonding diagram for a packaged die. In this case four legs are available for grounding which may suggest a low value of common lead inductance.

The problem with common lead inductance is that at RF frequencies it doesn't require very much before serious problems arise. Any common lead inductance in a packaged die equates to series inductive feedback between each and every non grounded package pin. This limits the isolation which can be achieved between pins, which can seriously degrade the performance benefits of using external filters and can have disastrous de-stabilising effects in the case of re-entrant gain structures such as amplifiers. Figure 10 is plot of the maximum isolation which can be achieved, versus frequency, in packages having common lead inductances of 0.25nH, 0.5nH and 1nH.

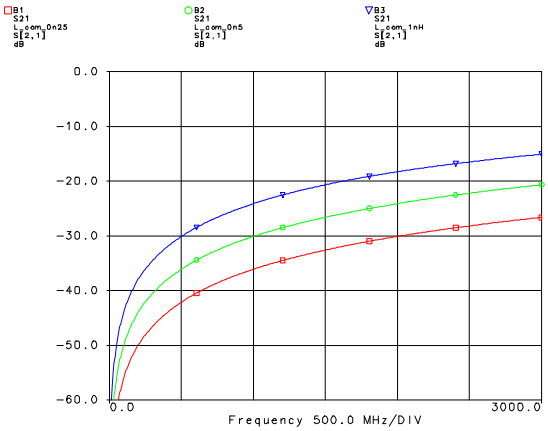

Figure 10: Isolation across a package versus frequency for varying values of common lead inductance

the bonding configuration shown, four pins devoted to RF grounding, this would amount to around 0.25nH of common lead inductance. Such a packaging configuration would not be of much use above about 2GHz.

One of the most cost effective ways of reducing the common lead inductance is to use a custom lead frame. A number of leads could then be directly connected to the die attach area, as shown in Figure 11.

Provided enough pins are devoted to RF grounding, a custom lead frame can often reduce the common lead inductance to an acceptable level. At higher operating frequencies, even lower common lead inductances are required. In this case some form of metal based package must be adopted or alternatively, the die can be mounted directly on the board. Another technique, which has been used successfully at frequencies in excess of 5GHz [11], is to use Multi-Chip Modules (MCMs)

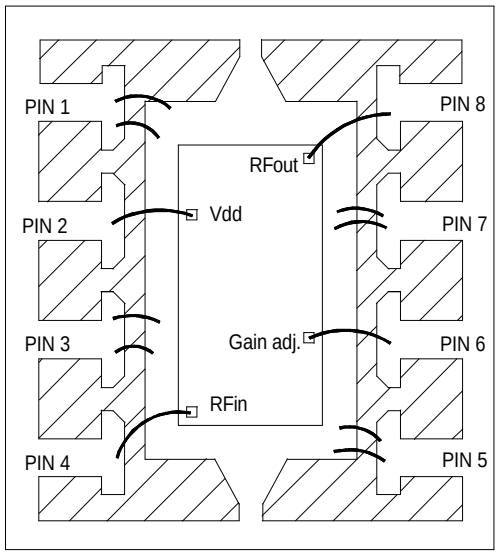

Figure 9: Packaged die bonding diagram

Even with just 0.25nH of common lead inductance the isolation is reduced to 30dB by 2GHz, whilst with 0.5nH of common lead inductance the isolation is reduced to 23dB. If a 20dB gain amplifier were placed in a package with just 23dB of isolation between input and output, the effect on performance would disastrous. It should be noted that a small outline package, such as an SOIC-8, bonded as shown in Figure 9, would have in the region of 1nH of inductance per leg bonded to the die attach area. For

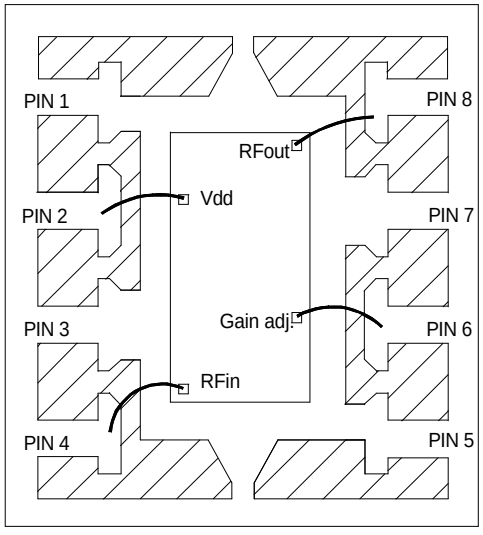

Figure 11: Example of a custom lead frame

One important aspect of packaging which has not yet been discussed is the thermal implications. A power amplifier, such as Anadigics' AWT0904 for GSM handsets, can be dissipating in excess of 2W of power. Although most RF ICs are likely to dissipate significantly less power than this, the thermal design of the IC and packaging must be considered.

Knowing the maximum junction temperature (Tj_{max}), the maximum ambient temperature at which the device must operate ($Tamb_{max}$), and the maximum power the IC will dissipate ($Pdiss_{max}$), then the maximum junction to ambient thermal impedance (ϕ_{JAmax}) which can be tolerated can be calculated, as shown in (1).

$$\Phi_{JA\max} = \frac{Tj_{\max} - Tamb_{\max}}{Pdiss_{MAX}} \qquad (1)$$

The total thermal impedance (ϕ_{JA}) is the sum of the junction to die attach (ϕ_{JB}), the die attach to case (ϕ_{BC}) and the case to ambient (ϕ_{CA}). The value of ϕ_{JB} is determined mainly by the process. Reducing the substrate height will improve it and clustering the higher current devices can degrade it but it is largely something which is fixed. The value of ϕ_{CA} can be improved by the use of external heatsinks or external air flow but these options are not always practical. The value of ϕ_{BC} depends critically on the package design and can be reduced.

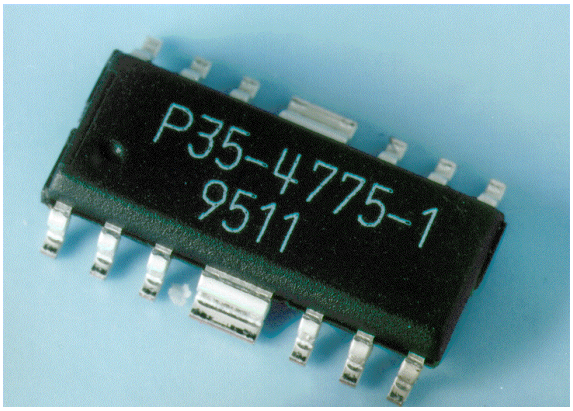

Figure 12: Thermally improved custom lead frame (Courtesy of GMMT)

One means of reducing ϕ_{BC} is to use a custom lead frame with adjacent pins connected to the die attach area. These pins can then be fused together to form a much wider pin, often referred to as a "bat-wing". Figure 12 is an example of this style of package, used in GEC-Marconi's P35-4775-1, a 2.2 to 2.7GHz amplifier which has a +22dBm output power capability.

Metal based ceramic packages have traditionally been used to provide very low thermal impedances. However these tend to be significantly more expensive than plastic, a fact which does nothing to foster their use within the competitively priced wireless components market. However, plastic packages with a copper slug attached to the underside of the leadframe die attach area have recently become available [12]. The base of the slug/package is then soldered to the board RF ground. This significantly reduces the package thermal impedance and also improves the electrical performance by drastically reducing the common lead inductance.

Summary

This paper has detailed some of the techniques which are used in the design of RF ICs for high volume applications. The best technique to ensure an RF IC is widely used in commercial wireless products is to make it very cheap. This means keeping the die size small, the processing simple and the packaging inexpensive. Once the part is cheap enough, the designers of commercial wireless products will start to consider it's technical merits.

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