# Design Trade-offs for High Linearity pHEMT Switches

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## Abstract

*This paper describes design trade-offs for high linearity GaAs SPDT switches suitable for operation with low control voltages. Typical applications for such devices include GSM handsets and WLAN transceivers. Parameters investigated include gate topologies, the use of drain-source bypass resistors and the use of external reference voltages. At 1.9GHz the best performing of the family of switch designs yielded a typical insertion loss of 0.58dB, isolation of 21.3dB, +36dBm 1dB compression point, +53dBm input referred 3rd order intercept point, and harmonic levels less than -80dBc.*

## Introduction

GaAs pHEMT processes have become the industry choice for the realisation of high linearity RF switches (Ref. 1). The paper details the design and measured performance of Single Pole Double Throw (SPDT) switches realised on a commercially available, low-cost pHEMT process. More specifically the paper will describe the measured effects of three design trade-offs:

- The topology of the pHEMT (i.e. The unit gate width and the number of gate fingers, for a given total gate width)
- The use (or not) of drain-source bypass resistors
- The use (or not) of an external reference voltage

A family of switches was designed by Plextek, using the 0.5µm pHEMT switch process of GCS Inc. (Ref. 2), in order for the above criteria to be analysed. The process is very simple, requiring just six masks, which allows the fabrication of very low cost components in high volume production.

## Switch Design

A set of similar SPDT switches covering DC to 2.5GHz has been designed. In each switch, each branch consists of three series connected pHEMT devices. Four variants of the switch have been fabricated and evaluated. These are switches with gate widths of 5x360µm and 9x200µm, both with and without drain-source bypass resistors (of value 2kΩ). In addition to this, each of the switches can be operated with or without a reference voltage. The schematic for the switches without the drain-source resistors is shown in Figure 1, and that for the switches with drain-source resistors in Figure 2. The (optional) external reference voltage is represented by V(+). The four variants are shown in GDSII layout format in Figure 3.

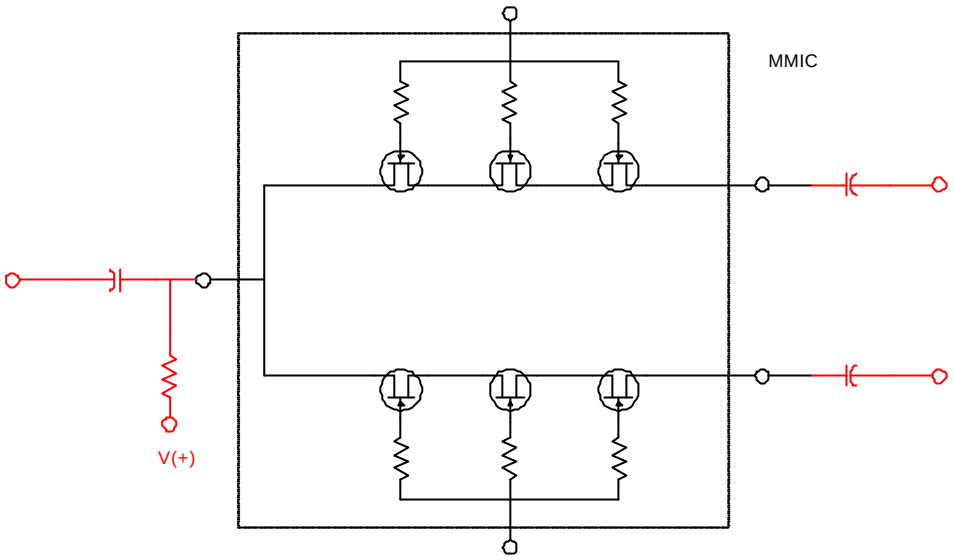


**Figure 1: First Variant of High Linearity SPDT Switch – No Drain-source Bypass Resistors**

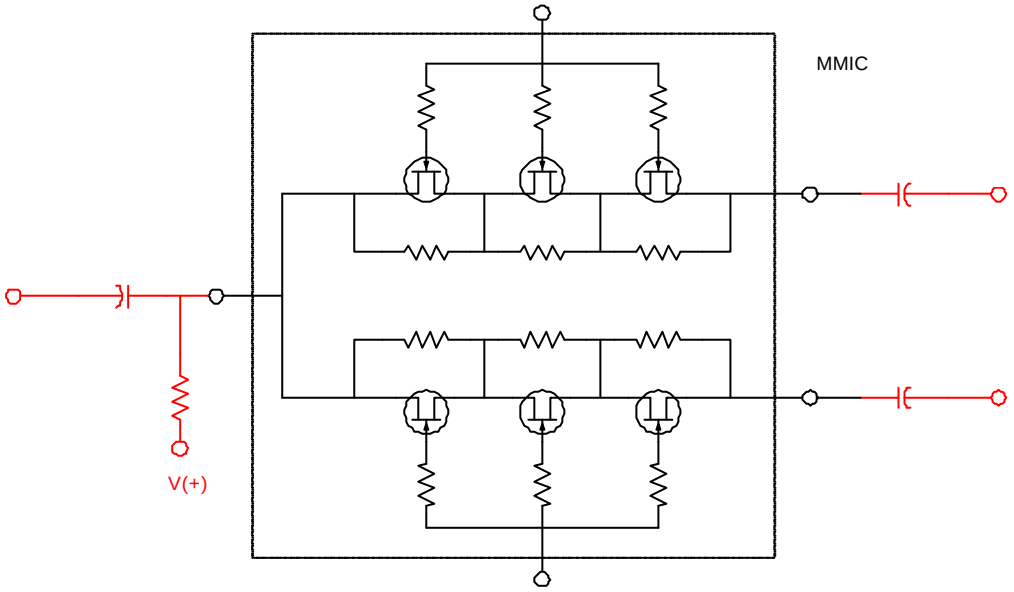


**Figure 2: Second Variant of High Linearity SPDT Switch – With Drain-source Bypass Resistors**

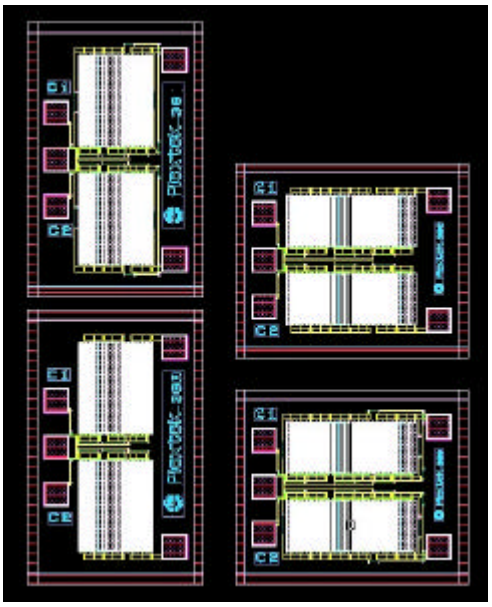

**Figure 3: Layout of all four MMIC Variants**

A photograph of one of the switches, namely the one using 5x360µm devices, with drain-source bypass resistors, is shown in Figure 4.

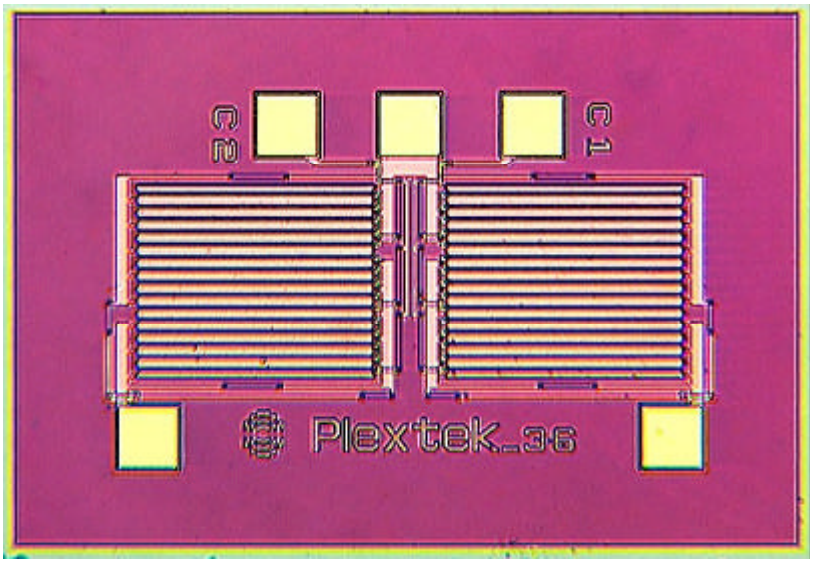


**Figure 4: Photograph of the High Linearity SPDT Switch**

## Switch Evaluation

The switches were tested (as wire-bonded bare die) on a Rogers 4003 PCB as shown in Figure 5. The switches operate using positive control voltages only, but do require external DC blocks at each RF port. These were realised using 0402 surface mount (SMT) capacitors. It is also possible to operate the switches with a reference voltage (equal to the positive control voltage) on the RF ports. If required, this reference voltage is applied to the common port via a 3KΩ 0402 SMT resistor.

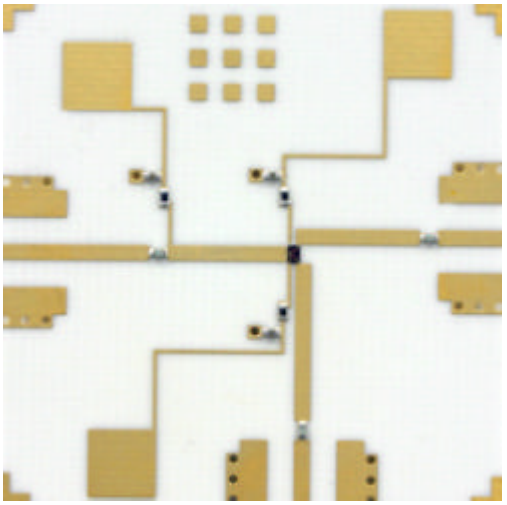

**Figure 5: Photograph of Switch Evaluation PCB**

Each switch was evaluated using 0 and xV complimentary control, where x is a positive voltage, and can vary from as low as 2V to as high as 8V. (The nominal operating value was +3V). Each switch was tested with and without a reference voltage. A selection of the results is summarised in Table 1. In this table, control voltages of 0 and +3V were used, and therefore the reference voltage (when used) was also +3V.

| Reference Voltage | Drain-source bypass resistors | Gate width | Insertion loss at 1.9GHz | Isolation at 1.9GHz | P-1dB at 1.9GHz | 2nd Harmonic of 1.9GHz | IP3 at 1.9GHz |
|---|---|---|---|---|---|---|---|
| With Vref | With Rds | 5x360µm | 0.58 | 21.3 | 36.0 | -80 | +53.0 |
| | | 9x200µm | 0.58 | 21.4 | 35.3 | -80 | +54.0 |
| | Without Rds | 5x360µm | 0.78 | 20.2 | 36.0 | -80 | +50.0 |
| | | 9x200µm | 0.77 | 20.2 | 35.3 | -80 | +51.0 |
| Without Vref | With Rds | 5x360µm | 0.56 | 21.1 | 35.3 | -72 | +52.5 |
| | | 9x200µm | 0.56 | 21.2 | 35.0 | -69 | +53.5 |
| | Without Rds | 5x360µm | 0.78 | 20.1 | 34.3 | -73 | +50.5 |
| | | 9x200µm | 0.76 | 20.2 | 34.2 | -70 | +51.5 |

**Table 1: Comparison of measured performance (0/+3V)**

A typical small-signal performance measurement is presented in Figure 6. In this case the 5x360µm variant with both drain-source bypass resistors (Rds) and a reference voltage (Vref) is shown. It can be seen from Table 1 that the unit gate width and the use of a reference voltage have very little effect on the small-signal performance. The biggest effect comes from the use of the drain-source bypass resistors. In this particular example the insertion loss is improved by the order of 0.2dB (see Figure 7) and the isolation by the order of 1dB

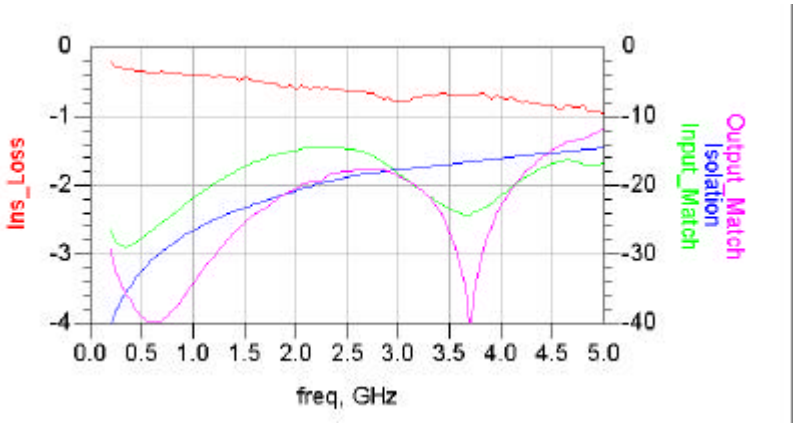


**Figure 6: Small-signal performance of 5x360um SPDT with Rds & Vref (0/+2.7V Control)**

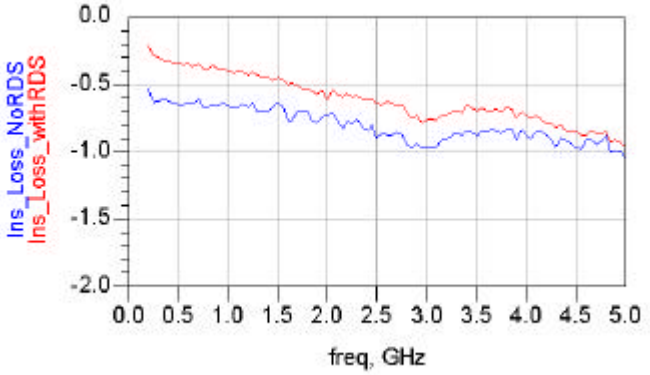


**Figure 7: Comparison of Insertion Loss of 5x360um SPDT, with and without Rds**

The 1dB power compression point measurement for the 5x360µm version, with Rds and reference voltage, and 0/+3V control is shown in Figure 8. The use of 5x360µm fingers rather than 9x200µm, and the use of the drain-source bypass resistors can both improve the output power compression performance by the order of 0.5 to 1dB. At a given frequency, the use of the reference voltage improved the performance by at least 1dB, as illustrated in Figure 9.

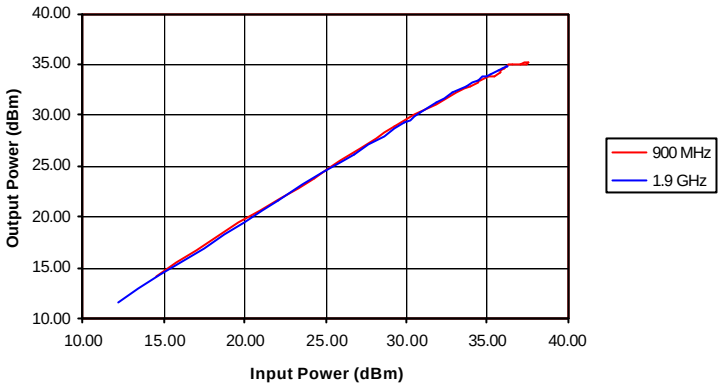


**Figure 8: Output Power Measurement of the High Linearity SPDT Switch**

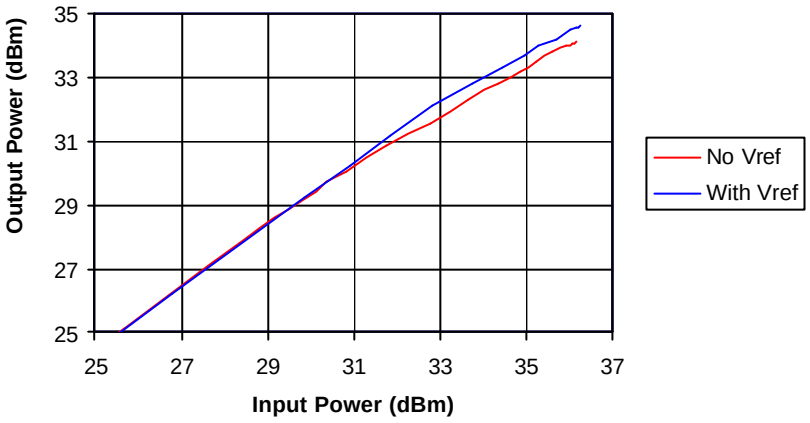


**Figure 9: Comparison of P-1dB of 5x360um SPDT, with and without Reference Voltage (3V)**

The switches utilising 9x200µm devices have 3rd order intercept points some 1dB higher than the equivalent 5x360µm switches. The use of the drain-source bypass resistors was shown to improve the performance by a further 3dB. The use of a reference voltage was shown to have very little effect at positive control voltages of 3V and above. However, at very low control voltages (for example 2V) the use of the reference improves the figure by 13dB, as illustrated in Figure 10 and Figure 11. The nominal performance of the 5x360µm version, with Rds and reference voltage, and 0/+3V control is shown in Figure 12. Here the input referred 3rd order intercept point is +53dBm

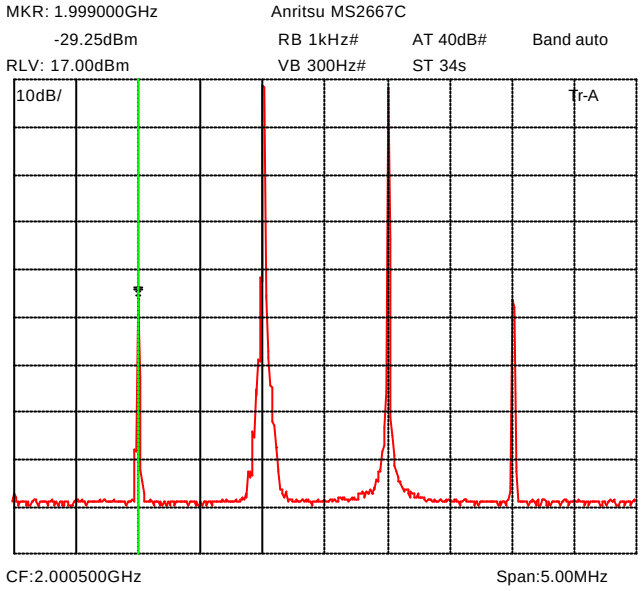


**Figure 10: Intermod Performance at 0/+2V Control, No Reference Voltage**

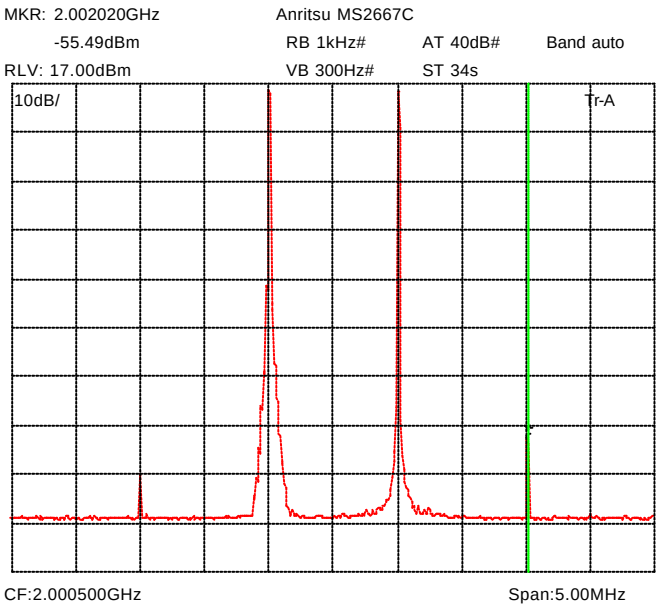


**Figure 11: Intermod Performance at 0/+2V Control, With +2V Reference Voltage**

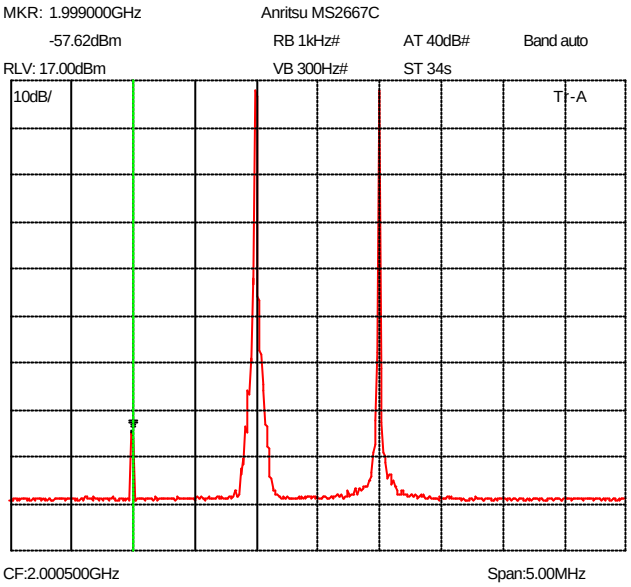


**Figure 12: Intermod Performance at 0/+3V Control, with +3V Reference Voltage**

The gate-finger configuration, and the use of drain-source bypass resistors have very little effect on harmonic performance, as shown in Table 1. The use of an external reference voltage, however, improves the performance by the order of 10dB

## Conclusions

Switch measurements have shown that the use of a different number of gate fingers for a given total gate width (in our example, 1800µm) has very little effect on either the small or large-signal performance of a SPDT switch at frequencies up to 2.5GHz. The use of on-chip drain-source bypass resistors improves the small-signal insertion loss and isolation by 0.2 and 1dB respectively. The use of an external reference voltage on the drains/sources of the pHEMTs has an important effect on the non-linear performance of the switch. For a given device and control voltage, the use of an external reference improves the power handling by the order of 1dB, and the harmonic rejection by the order of 10dB. The reference voltage also improves the third order intercept point, but only at low (~ 2V) control voltages.

In summary, of the design trade-offs considered, the following are the most important in achieving optimum performance for high linearity pHEMT switches:

- Include drain-source bypass resistors
- Use an external reference voltage

## References

1. "The Design of Integrated Switches and Phase Shifters"
   Liam Devlin, IEE Colloquium on The Design of RFICs and MMICs, November 1999.

2. http://www.gcsincorp.com/services/Phemt.htm