The Future of MM-Wave Packaging

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Abstract

The mass market for consumer wireless products led to the development of low cost packaging technology suitable for use at RF frequencies. As the market developed there was a drive for miniaturisation that helped reduce package parasitics, which assisted in pushing up the maximum operating frequency. ICs are now readily available in Surface Mount Technology (SMT) packages with maximum operating frequencies of around 40 to 45GHz. Further development work is now on-going to push the upper operating frequency of SMT packaged MMICs still higher. Of particular interest is SMT packaging for use at V-band (to address the ISM bands around 60GHz), for automotive applications at 77GHz and 79GHz and for E-band applications at 71-76GHz and 81-86GHz. This paper discusses the challenges of meeting these requirements and looks at the potential approaches that could be used to address them. It is based on an article originally written for Microwave Journal and published in February 2014.

1 Introduction

The most popular package style for microwave frequency ICs is the QFN (Quad Flat pack No-leads). Figure 1 is a photograph of a bare die microwave amplifier MMIC and two QFN packaged parts containing the same die type. The exposed paddle on the underside of the QFN package is normally the ground connection and is connected to the backside of the die. It is clear that the use of the bare die would still offer the ultimate in size reduction but the use of an SMT packaged component means that assembly and handling is comparatively straight forward. This allows reduced product cost for high volume applications and is why so much effort is being devoted to extending the frequency range of SMT packaging to still higher mm-wave frequencies.

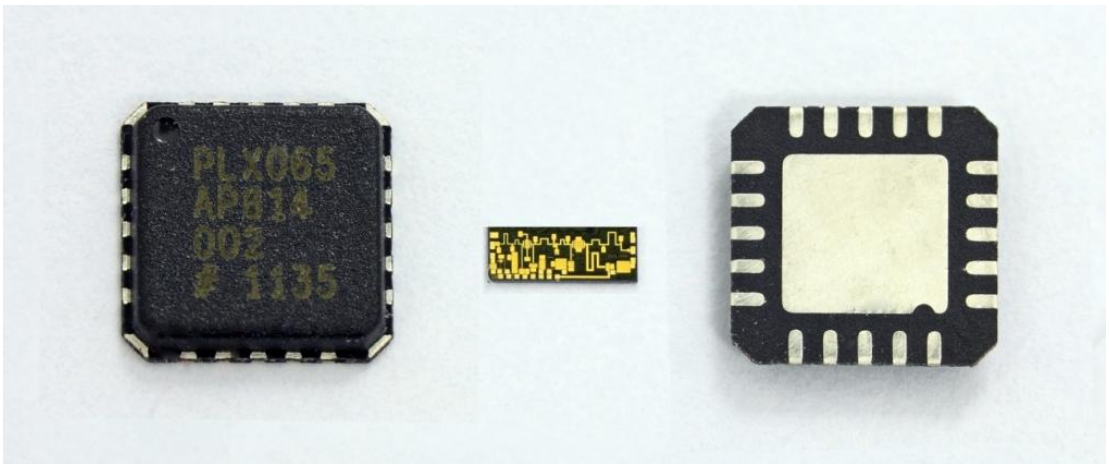

Figure 1: Microwave amplifier IC, QFN packaged and bare die

For frequencies up to around 20GHz, traditional over-moulded plastic packaging is normally used. In this case the plastic moulding compound is in direct contact with the surface of the die. As operating frequencies increase air-filled plastic cavity packages also start to be used and at still higher frequencies laminate or LCP (Liquid Crystal Polymer) [1] based packages can be used to achieve optimum performance whilst still retaining the same QFN footprint [2].

The two biggest challenges in SMT packaging of mm-wave ICs are tolerating the series inductance of the RF signal bonds and tolerating the overall grounding inductance (IC, package and PCB). With QFN

packaged microwave ICs the solid metal base provides a low grounding inductance for the package itself. The grounding inductance of the PCB, which often dominates, is minimised by:

- Using an array of ground vias providing a low inductance path from the package base to the PCB ground
- Specifying a suitably thin PCB material to reduce the inductance to the PCB ground
- Using Grounded Coplanar Waveguide (GCPW) with close ground to signal line coupling

The effects of package grounding are discussed in more detail in [3].

The approach used to tolerate the series inductance of the RF bond from die to package pin is to absorb it into a low pass filter structure [3]. Provided the inductance is adequately low then the package lead-frame and PCB land pattern can be adjusted together with the bondpad on the IC to provide effective shunt capacitances of suitable values for a well-matched low loss transition.

The absolute value of the series inductance that can be absorbed into such a low pass filter dictates the maximum frequency to which this approach can be adopted. An inductance of 0.2nH can be absorbed into a 50Ω matched, third order low pass filter with a cut-off frequency of around 45GHz and this is essentially the upper frequency limit for SMT packaging of ICs using a conventional wire-bonded approach.

To allow operation beyond 45GHz new packaging approaches need to be developed, which either significantly reduce or avoid the effects of series RF bond inductance and grounding inductance. The following techniques provide a means of doing this and have all been successfully demonstrated as options for SMT packaging of ICs at high mm-wave frequencies:

- Packages with waveguide (WG) apertures
- Packages with integral antennas
- Micro-coax based packaging
- Packages using “hot-vias”
- Flip-chip Wafer Level Chip Scale Packaging (WLCSP)

Each of these approaches is described in more detail below.

2 Packages with WG Apertures

Various techniques exist for transforming from waveguide to microstrip or Grounded Coplanar Waveguide (CPW) [4]. The most compact approach is to use a probe transition. A probe normally extends through the broad wall of the waveguide and is positioned one quarter of a wavelength from a back-short (a waveguide short-circuit). The incoming RF signal is reflected from the back-short with a phase inversion. The reflected wave therefore adds coherently with the incident (incoming) wave at the location of the probe creating a voltage maximum. This generates an RF signal in the probe, which is passed through the broadside wall of the waveguide.

Such transitions are commonly used in transceiver modules [5] and, at high mm-wave frequencies, the required dimensions are such that they can be incorporated into an SMT package to provide a waveguide aperture for reception and/or transmission of the mm-wave signals.

Figure 2 is a cross-section of a novel SMT package to waveguide transition taken with permission from [6]. The packaged component is a 77GHz transmitter for automotive radar, which is mounted onto a PCB motherboard with a WR12 waveguide output on the underside. Chip #1 is the automotive radar MMIC; chip #2 is the transition realised as a printed structure on an organic PCB material.

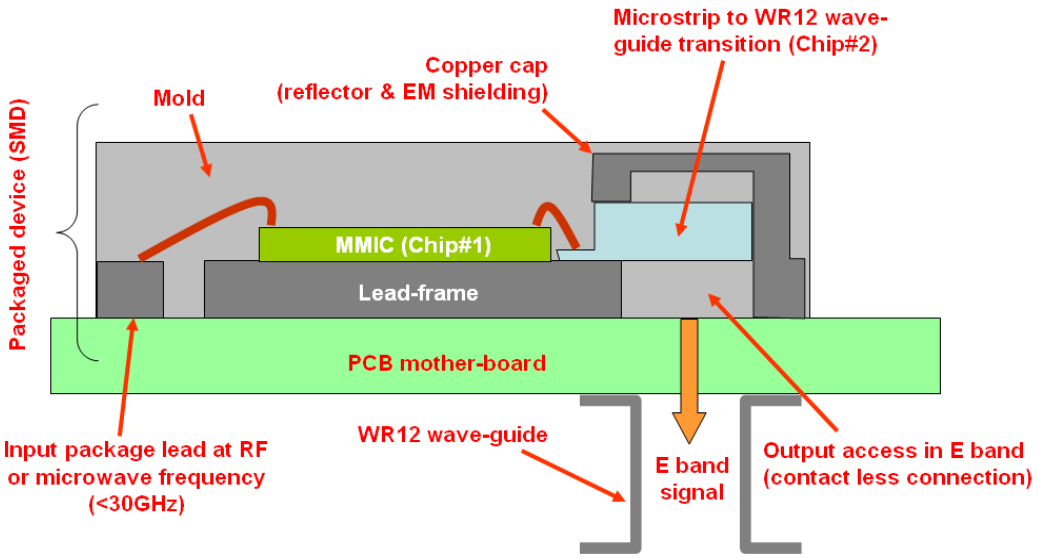

Figure 2: Formation of 77GHz SMT package with WG aperture (courtesy UMS)

The transition described in [6] demonstrates an insertion loss of 1.2dB for a single transition at 77GHz, based on evaluation of a back-to-back test piece. For the MMIC assembled into the WG package, the measured transmit power drops by 3dB compared to that measured on wafer. This is mainly attributed to the wire-bonded transition from the probe substrate (chip #2) to the MMIC (chip #1) which had not yet been optimised. A photograph of both faces of the 9 x 6mm QFN package is shown in Figure 3.

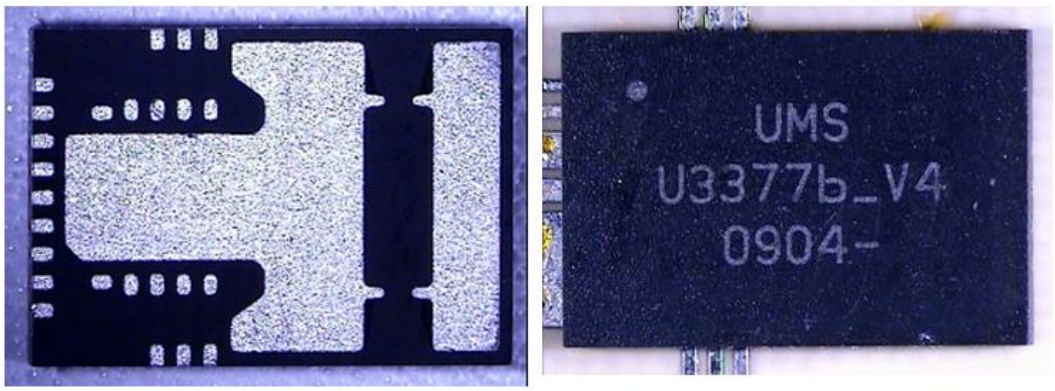

Figure 3: Photograph of plastic SMT package with integral WG aperture (courtesy UMS)

Although the use of plastic packaging technology significantly reduces the cost of this style of package compared to previous ceramic versions, it is still significantly higher than conventional packaging in SMT plastic QFN packages.

3 Packages with Integral Antennas

Rather than attempting to develop a package with a mm-wave SMT interface, or a waveguide aperture as described above, another alternative is to integrate the antenna into the package. Variants of this approach using both single antenna elements and multiple antenna elements (antenna arrays) have been demonstrated [7]. In both cases all other interfaces to the IC are SMT with the integral antenna forming the mm-wave transition. This approach is only possible at high mm-wave frequencies where the required physical size of the antenna becomes sufficiently small.

One of the most impressive demonstrations of this approach to date is a W-band phased array transceiver from IBM [8]. Four 16-element transceiver ICs were integrated into a single package containing 64 radiating elements. Figure 4 is a photograph of the package showing the antenna array. The spacing between the elements is λ/2 at 94GHz (around 1.6mm). The spacing from the edge antennas to the side of the package is λ/4, which facilitates the tiling of multiple components to realise a larger array. The design targets radar and active imaging applications where small size and low weight are required.

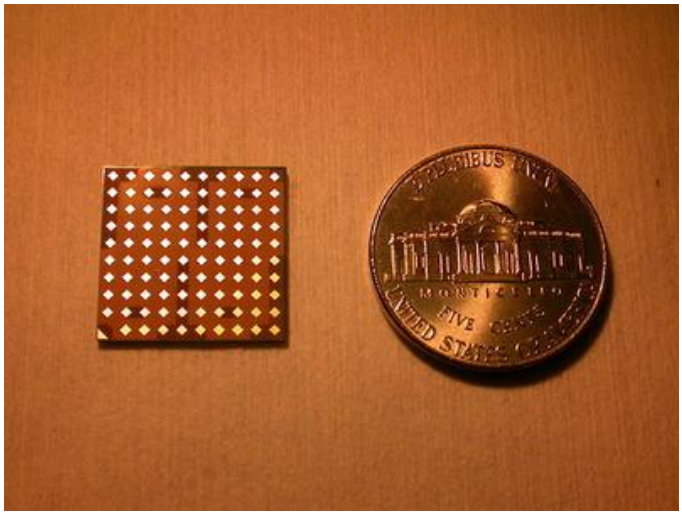

Figure 4: Photograph of 94GHz SMT transceiver with integral antenna array (courtesy IBM)

A photograph of one of the 16-element die is shown in Figure 5. It contains 32 receive channels (to facilitate simultaneous reception in two polarisations) and 16 transmit channels (which can be switched to either polarisation).

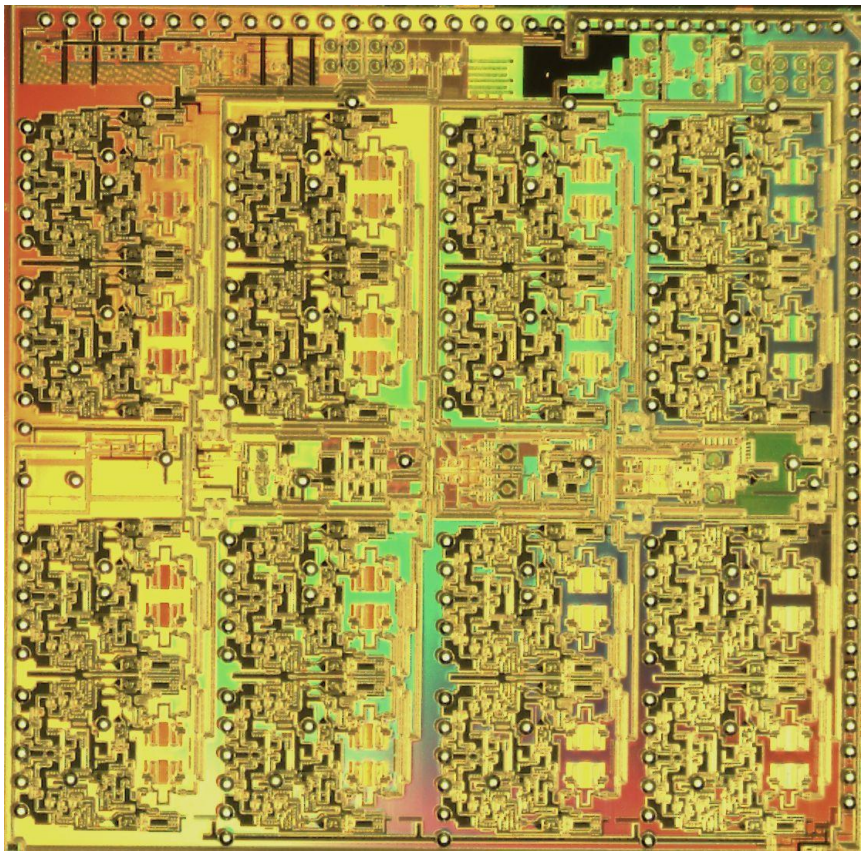

Figure 5: Photograph of 94GHz multi-element transceiver IC (courtesy IBM)

The radiating patches on the package are not in direct contact with the IC. A good description of the approach that is used is provided in [8], which describes a 60GHz antenna in package array. A cross-section of the package PCB stack-up is shown in Figure 5. A feed line from the IC couples to the radiating patch through an aperture in the antenna ground plane. A reflector positioned beneath the antenna feed line is also connected to the antenna ground plane. The package solution described in [8] uses an LCP core surrounded by woven-glass reinforced laminates with adhesives and is suitable for low cost, high-volume manufacture.

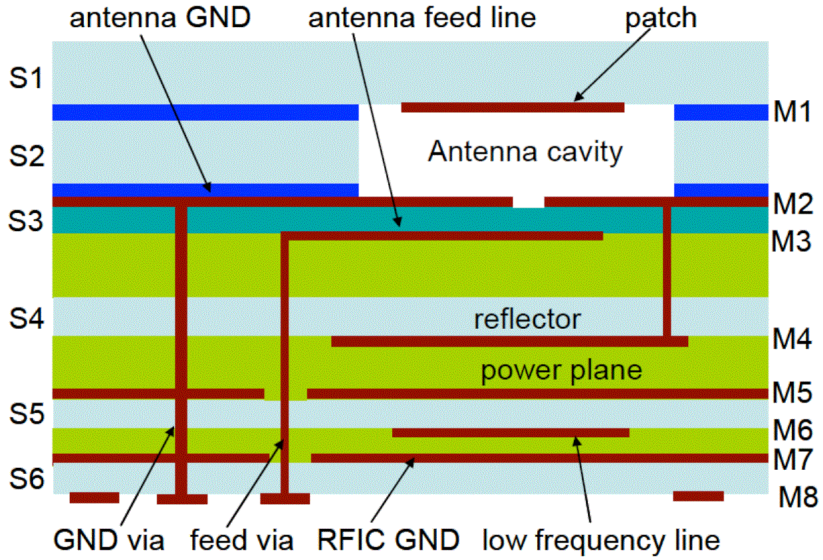

Figure 6: Cross-section of an integrated package antenna stack-up from [8] (courtesy IBM)

In addition to dispensing with RF bondwire inductance, the use of the multi-element antenna array has two other advantages:

- The total output power is the sum of multiple parallel transmitters so the available transmit power is increased
- The phase of the different elements can be adjusted to provide beam steering

The control of the amplitude of each transmitter also provides the possibility to shape the antenna pattern and even introduce nulls to avoid interferers.

One potential downside to this approach is that additional RF bandpass filtering cannot be included. However, the small size of the antenna means that it should provide significant rejection at low frequencies.

4 Micro-coax Based Packaging

Micro-coax packaging is an innovative and elegant approach to addressing the problem of RF bond inductance. The bondwire is transformed into a co-axial transmission line of controlled impedance (normally 50Ω) by the addition of a dielectric coating and then a grounded conductive outer. Accurate control of the dielectric constant and the thickness of the dielectric is required to set the characteristic impedance of the micro-coax transmission line.

The formation of the micro-coax transition, from [10], is depicted in Figure 7. The package assembly steps include:

A. Die attach and wire bond
B. Conformal dielectric coating
C. Laser cutting of vias to allow metallic contact
D. Selective metallisation of ground shield

Obviously some form of capping step would normally follow the above.

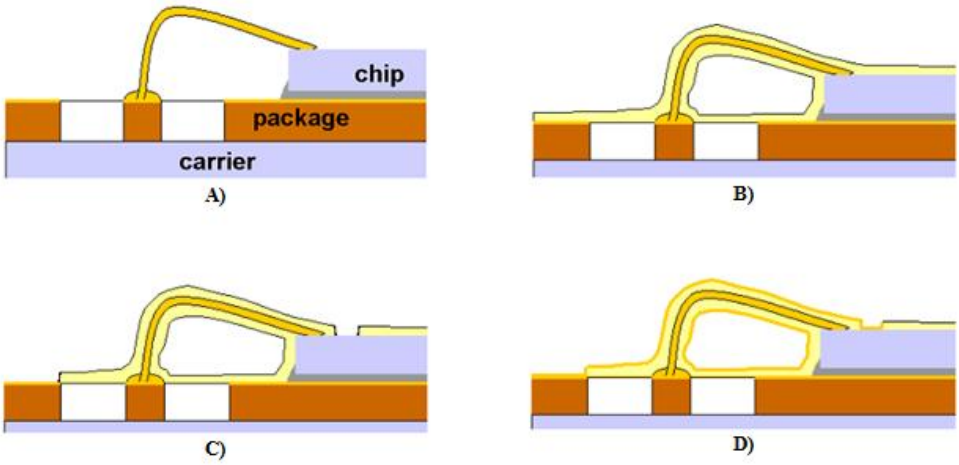

Figure 7: Formation of micro-coax interconnects (courtesy Bridgewave)

Figure 8 is a photograph showing micro-coax through line test pieces. The measured performance of a 2.2mm length of micro-coax is plotted in Figure 9 and shows an insertion loss of less than 0.7 dB at frequencies up to 115 GHz. The return loss is better than 20dB across most of this band with a worst case value of around 17dB at 60GHz.

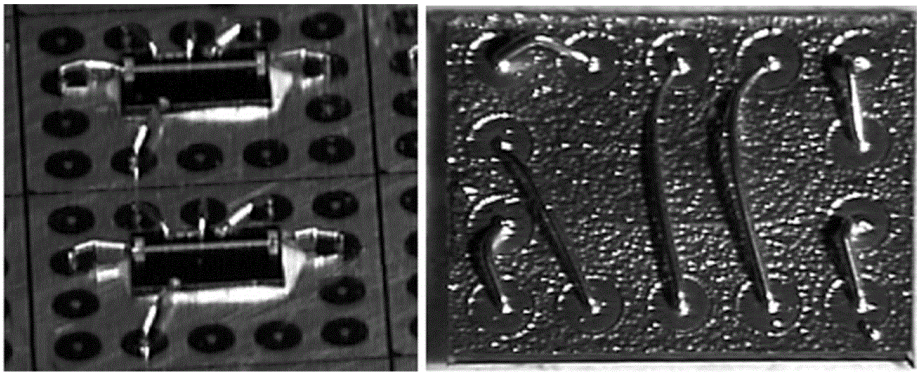

Figure 8: Photograph of micro-coax test links (courtesy Bridgewave)

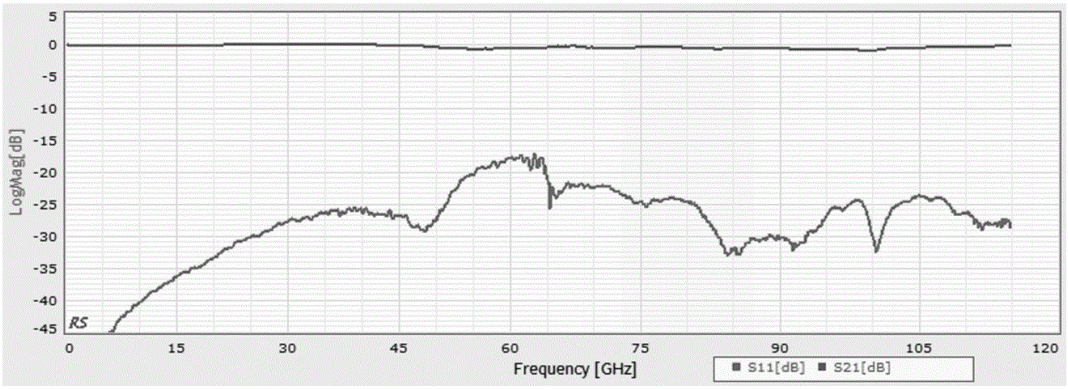

Figure 9: Measured performance of 2.2mm long micro-coax test link (courtesy Bridgewave)

Figure 10 is an X-ray photograph of an 18–31GHz LNA (CHA2069 from UMS) packaged using micro-coax technology. The coaxial structure of the interconnects is clearly visible, as are ground vias within the MMIC die. The measured performance of this part can be found in [10] and is very close to that of the bare die.

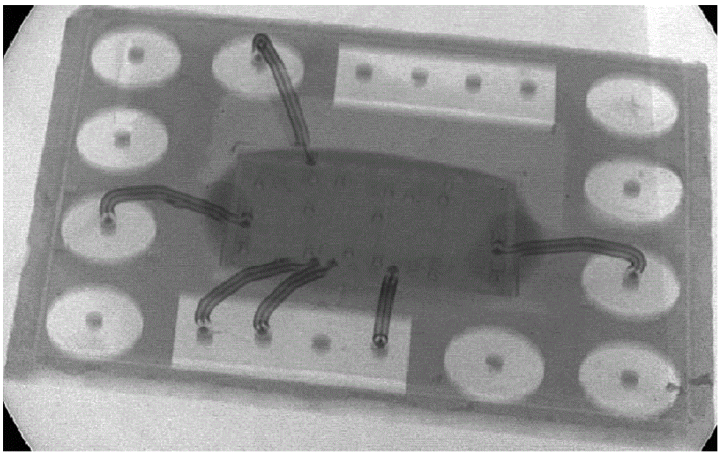

Figure 10: X-ray photograph of a micro-coax packaged LNA (courtesy Bridgewave)

The micro-coax approach depicted in Figure 7 and Figure 10 uses a coaxial feed-through. It has the benefit that it can be used to realise a hermetically sealed package but the downside is that it is not cost-effective for most consumer applications. In order to address this, a micro-coax/leadframe approach is described in [10], which allows for lower production costs. A QFN style package is used as a demonstration vehicle and good performance is demonstrated to 50GHz.

The micro-coax approach is a viable route to avoiding the effects of series RF bond inductance and as a transmission medium it has been demonstrated to show good performance to beyond 100GHz. However, there is still some uncertainty about its potential to provide a low cost packaging solution for use in the 50 to 100GHz range.

5 Packages using “hot-vias”

Most GaAs and GaN processes include a through substrate via capability. This provides low inductance interconnects from the front side of the die to the back. The effective inductance is dependent on the substrate height and via size but is typically around 20pH. In conventional MMIC designs the vias are used to provide low inductance ground points with the back side of the die being ground. If patterning of the back side metal is possible then some of these ground contacts can be isolated and can be used as low-inductance RF interconnects. This allows the die to form the base of a true chip-scale SMT package as depicted in Figure 11. The inductance of the RF interconnect has been reduced to around 20pH, which should in theory allow operation to beyond 100GHz.

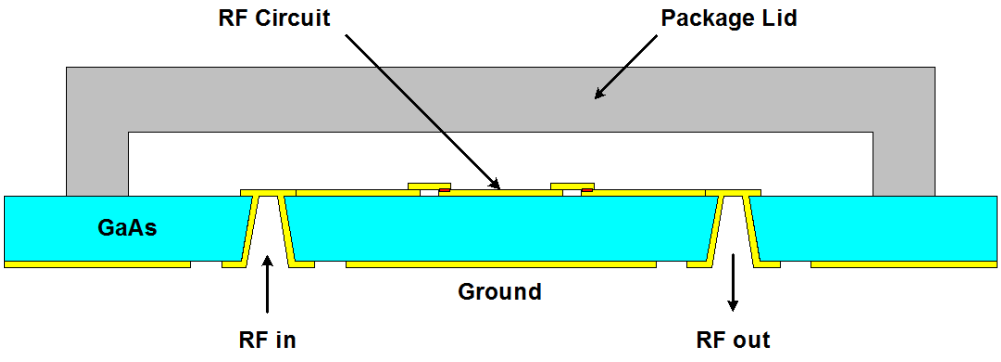

Figure 11: Use of "hot-vias" in SMT packaging

The hot-via packaging approach has previously been demonstrated [11] with measured through line test pieces indicating losses of 0.5dB at 45GHz for a single hot-via transition. The measured performance of a 15-30GHz amplifier IC, modified to allow hot-via packaging, is also presented in [11] and shows performance similar to that of the bare die.

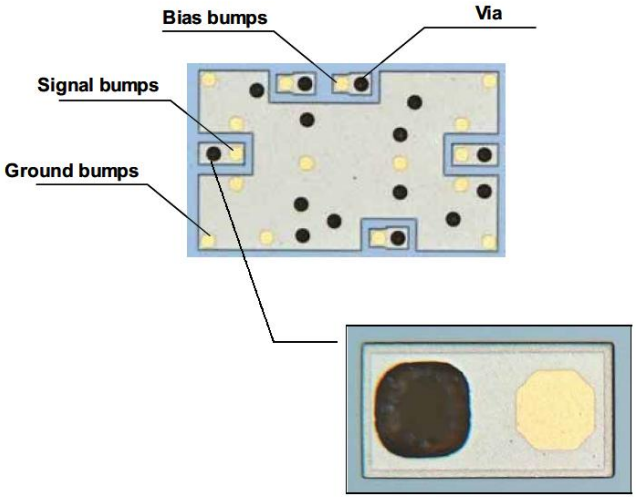

Figure 12: Photograph of backside of LNA IC using RF and DC hot-vias (courtesy UMS)

Avago has introduced commercially available parts in Wafer Scale Packages (WSP) that make use of hot-vias. Published data from Avago [12] suggests that the hot-via transition should work well up to 45GHz. However, at the time of writing the product range offered in this package style does not appear to extend beyond 12GHz.

It is clear that hot-via transitions offer a practical way to significantly reduce the series inductance of an IC to PCB transition. However, the technology has yet to prove itself practical for commercial use at mm-wave frequencies.

6 Flip-chip Wafer Level Chip Scale Packaging (WLCSP)

In Wafer Level Chip Scale Packaging (WLSP) the die is normally packaged in a ball grid array with the surface of the die facing down towards the PCB on which it is mounted. The resulting package is truly chip scale, being not much larger than the die itself. This approach provides miniaturisation and results in very low interconnect parasitics. WLCSP is often undertaken as an augmentation to the wafer fabrication process.

A number of manufacturers have WLCSP processes. Infineon's embedded Wafer Level Ball Grid Array (eWLB) technology [13] has been successfully used in its V-band and E-band transceiver products [14], which are about to be released as commercially available products.

Sumitomo has demonstrated a set of packaged E-band ICs in WLCSP [15]. These include a frequency tripler, an LNA, a balanced mixer and a Power Amplifier (PA). The packaging technology is depicted in Figure 13. The actual IC is GaAs PHEMT technology with additional processing steps to form the WLCSP. This includes the ability to add routing to connect to a uniform array of solder balls for SMT attach. The surface of the IC package is covered with a common ground metal, which has multiple links to the die ground. Openings are made in the package ground plane for signal, control and bias connections to the die.

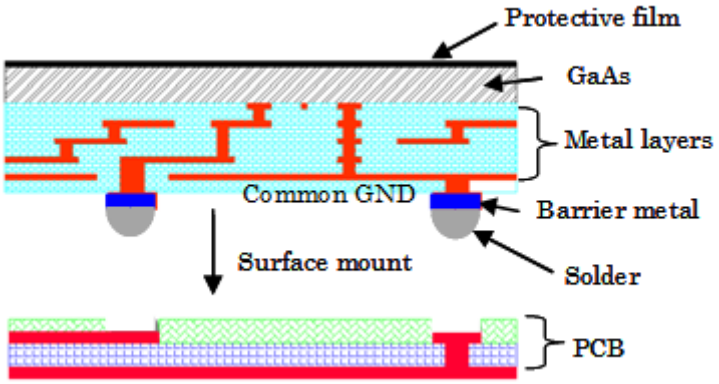

Figure 13: Cross-section of WLCSP approach (courtesy Sumitomo)

Figure 14 shows an example of one particular WLCSP part, an LNA. The packaged part was mounted on a PCB with a GCPW interface. The performance of the packaged part on the IC was measured with G-S-G probes, as would be used for RFOW evaluation. The comparison of the measured to modelled performance gives an honest indication of the degradation due to packaging. Each RF transition incurs an insertion loss of around 1.5dB.

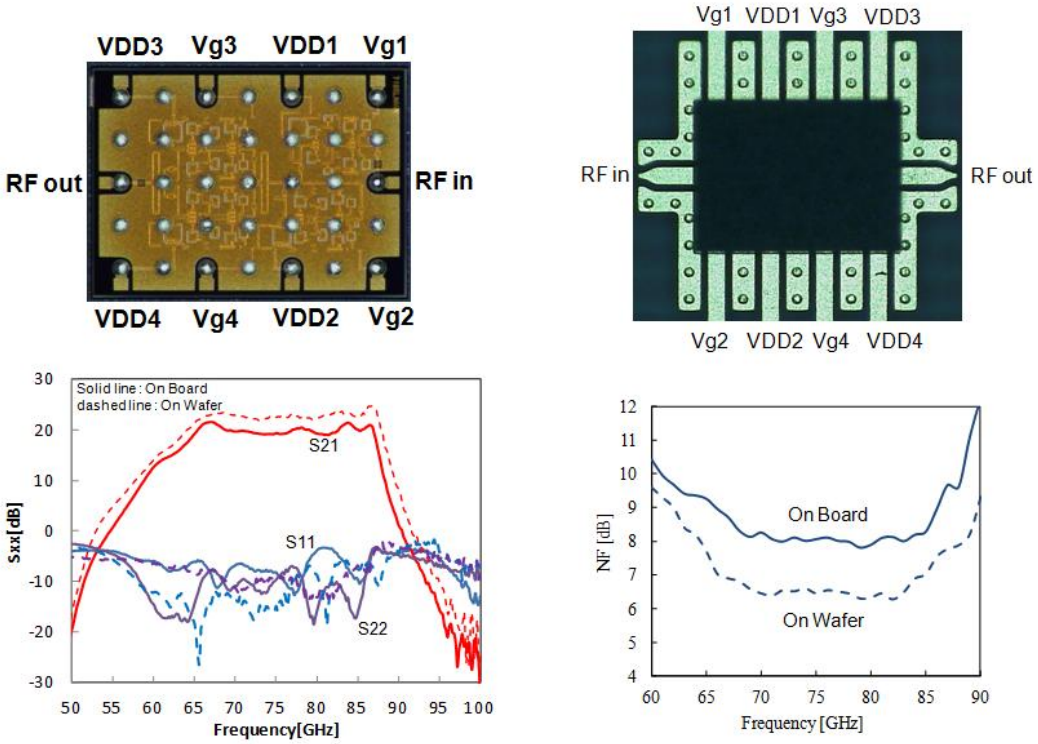

Figure 14: Example of E-band LNA in an SMT WLCSP (courtesy Sumitomo)

For ICs having net gain, with input and output at the same frequency (such as the LNA above), the effects of grounding inductance are much more significant than for transceivers. Great care must be taken to minimise the effective grounding inductance or severe performance degradation, or even instability, can result.

7 Summary and Conclusions

All of the packaging approaches described above have demonstrated their potential for use at frequencies to around 100GHz. However in the author's opinion there are two of these that are likely to see significant deployment in commercial products. These are the ICs with integrated array antennas and the flip-chip mounted ICs in WLCSP. Both have clear potential for low cost, high-volume production which is essential for adoption in consumer applications.

The integrated antennas avoid the problems associated with making a mm-wave SMT contact to a PCB. They also mean that the tolerable grounding inductance can be much higher. The use of an antenna array allows increased transmit power by in-air combination of multiple lower level signals and allows steering of the antenna beam. This approach is unlikely to be practical for longer range point to point links where higher transmit powers and antenna directivity would be required but it is very attractive for shorter range links and indoor communications.

Flip-chip WLCSP uses miniaturisation to keep package parasitics very low. The flip-chip mounting of the die means the path from the die to the PCB is minimised and bondwire inductance avoided. The parasitics of the PCB can still have a significant effect on the ultimate performance and co-design of IC, package and PCB is necessary to achieve optimum results. With complete receiver or transmitter ICs having only a single mm-wave port, the effects of PCB grounding inductance are significantly reduced but functional blocks such amplifiers must also tackle this issue as an integral part of their design and implementation.

8 Acknowledgements

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9 References

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