The Design of E-band MMIC Amplifiers

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Abstract

The worldwide availability of a large amount of spectrum at 71-76GHz and 81-86 GHz (commonly known as "E-band") for high data-rate wireless links has led to substantial interest. The design of electronic equipment at such high frequencies is challenging. Parasitic effects that were negligible at microwave frequencies become problematic and the availability of suitable active components is very restricted. The development of custom GaAs MMICs offers a route to realising low-cost, reproducible E-band components. This paper addresses the design and implementation of E-band MMIC amplifiers. It considers process selection, design challenges and practical approaches and presents the measured and modelled performance of a single-stage E-band gain block.

1. Introduction

The worldwide availability of a large amount of spectrum at 71-76GHz and 81-86 GHz (commonly known as "E-band") for high data-rate wireless links has led to substantial interest. The open access to such large amounts of spectrum directly leads to high demand for point to point links, providing they can be realised at a suitable cost. The availability of E-band components is currently very limited and the unit cost is far higher than that required to allow the realisation of low cost, commercial E-band links. However, the development of custom E-band GaAs MMICs offers a route to significantly reducing component costs and allowing the production of large quantities of E-band electronics at an adequately low cost.

This paper discusses the challenges of designing E-band MMICs. It covers process selection, design techniques and practical approaches and presents the measured and modelled performance of a demonstrator circuit, a single-stage E-band gain block.

2. Process Selection

The first consideration when choosing a process is to find a commercially available, qualified process that can offer useful gain across the E-band frequency range. Three categories of process have been identified that meet this initial requirement:

- 0.15µm or 0.13 µm gate length PHEMT
- 0.15µm gate length MHEMT
- 0.1 µm gate length PHEMT

Although CMOS and SiGe processes with transistors having high enough Ft to provide gain at E-band are also available, the GaAs processes above offer better NF and linearity. Acceptable NF and adequate linearity are essential requirements for point to point links and the processes identified are most suited to providing this. GaAs processes also have the advantages of a semi-insulating substrate and low inductance through substrate vias making higher levels of RF integration easier to achieve.

As the total gate width increases (more gate fingers and/or wider unit gate width) the parasitic effects increase (e.g. gate inductance and phase delay between gate fingers). This reduces the available high frequency gain of the transistors. Essentially on any given process the maximum useful device size is limited. Beyond this size the device does not provide an adequate level of gain for practical implementation of circuit functions (6dB is considered as the practical minimum). This is discussed in more detail below.

The most difficult requirement to satisfy when designing E-band amplifiers is output power capability/linearity. The maximum practical transistor sizes on the commercially available 0.15µm or 0.13µm gate length PHEMT processes results in relatively modest output power capability. Whilst

increasing the output power by combining multiple devices is obviously a possibility more gain is required to overcome the additional losses of the combiner networks. Increasing device count to achieve higher output power is thus a process of diminishing returns.

MHEMT processes offer more gain and slightly lower minimum NF than PHEMT processes of the same gate length. However their power density (output power per mm of gate width) is lower than for PHEMT processes and they are less suitable for the realisation of amplifiers requiring higher linearity or output power. Of today's commercially available GaAs processes the most appropriate choice for output power and linearity is the 0.1µm gate length PHEMT.

Another process feature that needs to be considered is substrate height (thickness). Most commercially available GaAs processes have a substrate thickness of 100µm. However some processes are available with a thinner substrate thickness of 50µm, which provides performance advantage at E-band. The advantage stems from the reduced via inductance inherent in the thinner substrate. The via inductance acts as series inductive feedback around the transistor and with larger transistor sizes this can degrade stability. This effect becomes more pronounced with increasing transistor size. This means that whilst the transistor might have higher "Maximum Available Gain" (MAG) the losses that must be introduced to ensure unconditional stability can reduce the practical gain that can be achieved to below the 6dB practical limit. This is discussed in more detail in the "Design Challenges" section below. A thinner substrate is therefore preferred for optimum realisation of E-band amplifiers.

With a 0.1µm gate length PHEMT having adequate breakdown voltage and a 50µm substrate height, it is estimated that an E-band amplifier with an IP3 of +34dBm would be practical. For optimum performance it is believed that separate design would be appropriate for the 71-76GHz and 81-86 GHz bands.

The demonstrator amplifier described in this paper was realised on the 0.15 µm gate length power PHEMT process of WIN Semiconductor (PP15-20). This was selected purely on convenience as space was available on a process run being undertaken primarily for different purposes. The process can be used for realising E-band amplifiers but is not necessarily the optimum choice.

3. Design Challenges and Approaches

Once the process has been selected detailed investigations into the design can commence. The example amplifier discussed in this paper was designed on the 0.15µm gate length Power PHEMT (PP15-20) process of WIN Semiconductors. This process is not suitable for particularly high output power or linearity at E-band. However, it is able to provide a useful level of gain and a process run was available on which to fabricate a demonstrator circuit.

The available gain of the PP15-20 transistors at E-band is marginal for the effective realisation of amplifiers. Care must be taken with selection of device size and bias point if the available gain is to be kept above the 6dB level that is considered the lower limit for practical circuit implementation. In order to choose the most appropriate bias point the effect of Vds bias on gain was evaluated. Figure 1 shows the effect of drain-source bias voltage (Vds) on maximum available gain (Gmax) and minimum NF for a fixed device size (2 x 50µm). It is clear that using a lower Vds results in lower NF. The effect of Vds on gain is modest above around 2.5V. Below this the available gain reduces with Vds.

The shape of the Gmax curves is also of interest. The kink in the response at around 48GHz marks the point at which the transistor transitions from being conditionally stable ($K<1$) to being unconditionally stable ($K>1$). At lower frequencies where the device is only conditionally stable Gmax cannot be determined and the gain response plotted is actually the MSG (Maximum Stable Gain). The MSG is a figure of merit that cannot be realised. If operated in this region some gain must be sacrificed to stabilise the transistor. By contrast, other than an allowance for the losses of matching components, something close to the Gmax can be achieved when the transistor is unconditionally stable.

The transition from a region of conditional stability at lower frequencies to a region of unconditional stability at higher frequencies is a well understood phenomenon. It happens because the gain of the transistor reduces with increasing frequency and eventually becomes low enough to ensure that the device is unconditionally stable. However, the gain curves of Figure 1 have another kink at or just above 80GHz (depending on Vds) where the transistor reverts back to being conditionally stable (or potentially unstable). This occurs because the reverse isolation is reducing with increasing frequency

(feedback is increasing). It only tends to happen in short gate length devices that have gain to very high frequencies. If processes are available on thinner substrate heights the grounding inductance for the transistor is reduced and the stability at high frequencies is improved. If a 3V or lower Vds is selected the transistor is unconditionally stable across the entire of the E-band frequency range, which is an attractive feature. Care must be taken if it is decided to select a transistor that is only conditionally stable in the band of interest. Additional MSG beyond the 6dB Gmax limit quoted earlier must be available to allow for the required gain sacrifice in stabilising the transistor.

The choice of Vds bias is obviously a compromise between linearity, NF, stability and available gain. This compromise must be reassessed once the choice of device size has been made as it is device size dependent. For the demonstrator amplifier presented here a 3V supply was selected with the transistor itself operating from a 2.7V Vds. Drain line resistors were included for out of band stabilisation (discussed in more detail later) and these were used to drop the 3V supply to the 2.7V level.

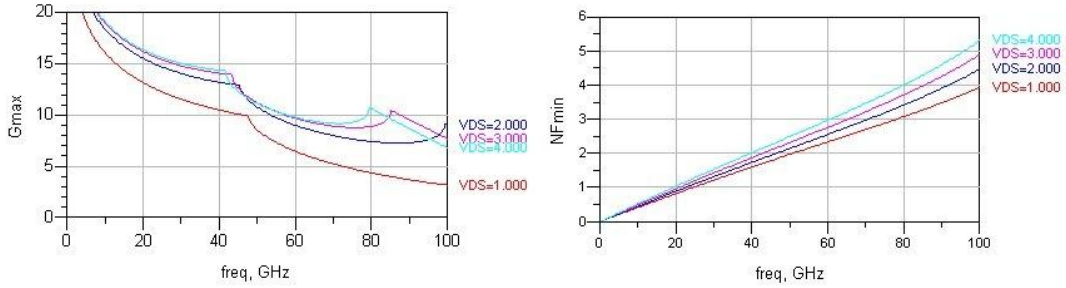

Figure 1: Simulated Gmax and NFmin for different Vds values (2 x 50µm transistor)

The next consideration is Ids bias. A 50% Idss bias (approximately -0.5V Vgs on the PP15-20 process) is the traditional class A bias point. Figure 2 shows the Gmax and NFmin for a 2 x 50µm transistor, biased at 3V Vds, as the Vgs is changed between -0.5V and -1V (approximately 50% and 20% Idss). Reduced current bias results in reduced Gmax and improved high frequency stability. A bias of 30% Idss (approximately -0.7V Vgs) was selected. It should be noted that there is some variation in typical Vgs with device size for a percentage Idss bias.

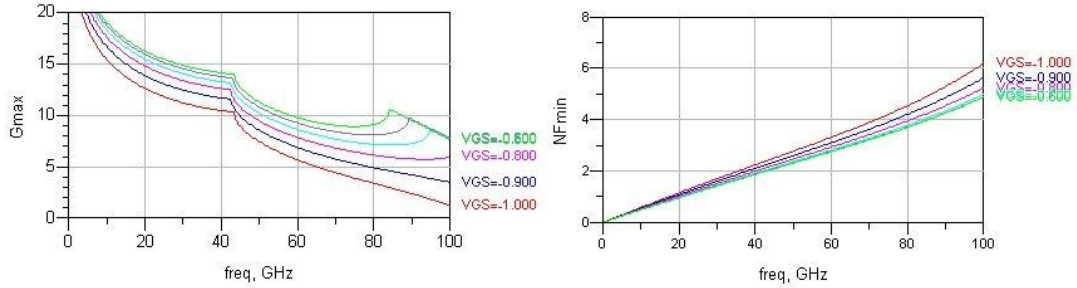

Figure 2: Simulated Gmax and NFmin for different Ids bias (2 x 50µm transistor at 3V Vds)

Having selected the device bias the next step is to select the device size. At E-band the challenge is to maximise the device size that can be used whilst retaining adequate available gain. Figure 3 shows the Gmax and NFmin for various unit gate widths (2 finger devices). Figure 4 shows the available gain and NFmin for various numbers of gate fingers (unit gate width fixed at 50µm). In all cases the transistors are biased at 3V Vds and 40% Idss. It is clear that increasing unit gate width decreases available gain and increases NFmin. Gain decreases because of distributed/parasitic effects and NFmin increases because of increased gate resistance. The most significant effect of increasing the number of fingers is to reduce the frequency at which the transistor reverts to a region of potential instability. Whilst it may appear that more device fingers offers the potential for additional gain this is unlikely to be the case once unconditional in-band stability is assured. For the demonstrator amplifier a 2 x 39µm device size was selected.

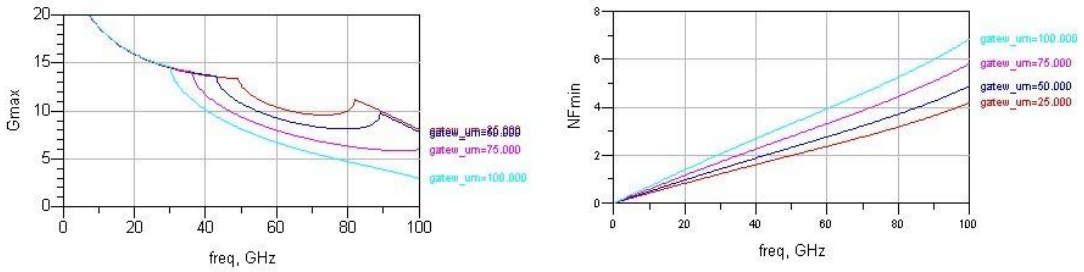

Figure 3: Simulated Gmax and NFmin for different unit gate widths (biased at 3V Vds, 40% Idss)

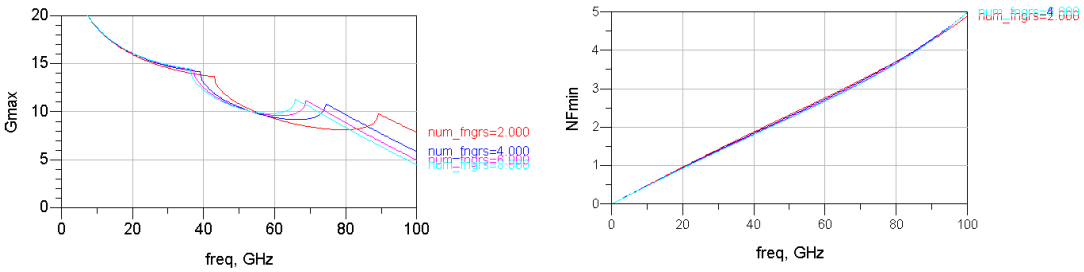

Figure 4: Simulated Gmax and NFmin for different number gate fingers (biased at 3V Vds, 40% Idss)

The Gmax and NFmin of the selected 2 x 39µm transistor biased at 2.7V Vds and 30% Idss is plotted in Figure 5. It can be seen that unconditional stability is exhibited across the entire of E-band. Potential instability is apparent above and below the operating band and the amplifier design must incorporate circuitry to ensure stability in this region. It can also be seen that the Gmax across E-band is only around 7dB. The amplifier design process is thus essentially an exercise in conjugately matching the transistor at input and output (and injecting the DC bias) whilst incurring as little loss as possible. Techniques such as matching for improved NF and linearity would cost gain and are luxuries that can only be considered at lower frequencies. This is essentially the case for all current commercially available processes capable of E-band operation.

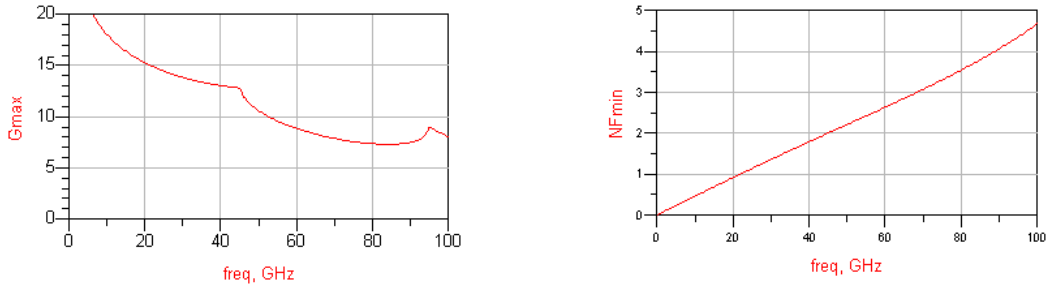

Figure 5: Simulated Gmax and NFmin for 2 x 39µm transistor biased at 2.7V Vds, 30% Idss

In addition to implementing simultaneous conjugate impedance matching at input and output, DC bias must also be injected. The bias networks can also be configured to provide losses above and below the operating band that ensure unconditional stability for the resulting amplifier at all frequencies. The first step in the design process was to implement the design using ideal components. Figure 6 shows the circuit schematic of the initial ideal component based design. Both input and output matching networks are essentially low pass structures. Series capacitors were also included for DC blocking but were optimised in value during the design process. At this stage the drain and gate bias chokes (L3 and L6) were ideal RF blocks.

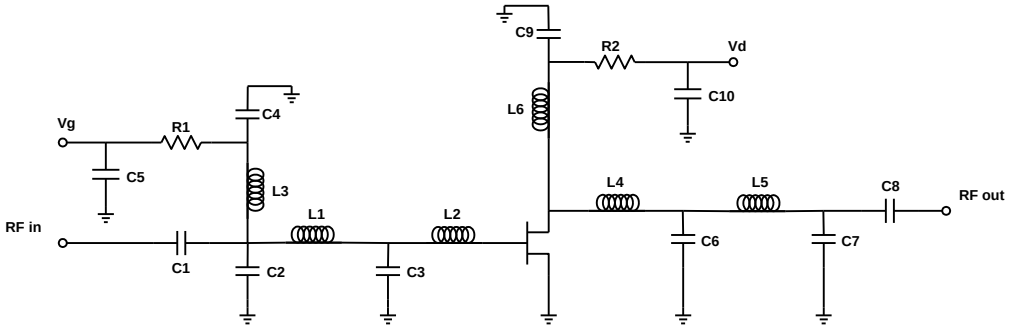

Figure 6: Schematic of single stage E-band amplifier (ideal matching components)

The simulated s-parameters of the amplifier with ideal matching components are shown in Figure 7. The next step was to determine how the ideal components could be implemented practically and to simulate the resulting performance.

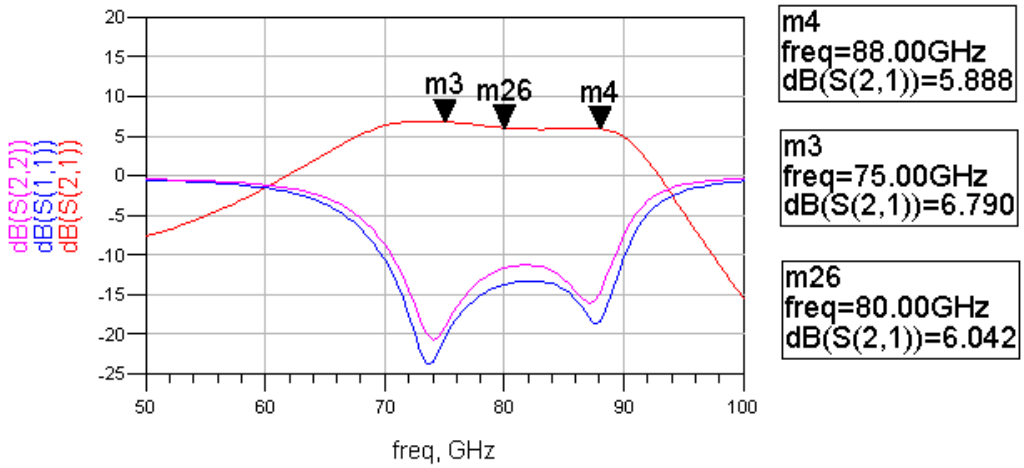

Figure 7: Simulated s-parameters of single stage E-band amplifier (ideal matching components)

The series inductors of the ideal implementation of Figure 9 are easily realised as short lengths of high impedance transmission lines. The inductor values are small and the required transmission line equivalents are very practical. The series capacitors are also easily realised as standard MIM (Metal Insulator Metal) structures. Whilst the shunt capacitors could also be realised as MIM capacitors the inductance of the through substrate vias is significant at E-band (20pH is 10Ω reactive at 80GHz) and has a considerable impact on the value of the shunt matching capacitors. When ideal capacitors and perfect grounding are used in the simulation (Figure 7) the largest value shunt capacitor is just 0.292pF. Allowing for the inductance of the vias reduces this and incorporating practical models for the MIM capacitors reduces it further to just 0.0654pF, which is just 9µm square. The concern was that variation in via inductance and capacitor size (value) with process spread could significantly modify the effective capacitance value. The approach used to address this problem was to realise the shunt capacitors (C2, C3, C6 and C7) as distributed transmission line structures (open circuit shunt stubs behave as capacitors at frequencies where their electrical length is less than λ/4).

The bias chokes used at gate and drain (L3 and L7 in Figure 6) were realised as high impedance shunt stubs of nominal length λ/4. The E-band short-circuit (realised using grounding capacitors C4 and C9) would thus be transformed to an open-circuit at the RF path. Bias can therefore be injected at the end of the λ/4 line without affecting the E-band performance of the amplifier. It is also convenient to use the bias networks at gate and drain to stabilise the transistor below band. Any transistor with available gain at E-band has substantial gain at lower RF frequencies and below. Resistors and lower frequency de-coupling can be introduced at the end of the bias stub to stabilise the transistor at lower frequencies. The stabilisation components are included in the schematic of Figure 6 (R1 and C5 at the gate side; R2 and C10 at the drain side).

The difficulty with implementing the bias network at E-band is that the MIM capacitor and via at the end of the bias stub does not provide a particularly good short circuit. The inductance of the via and the

electrical length of the MIM capacitors means that even a modest capacitor size, such as 0.5pF, looks inductive at E-band. An alternative approach that can be considered is to use a radial stub to realise a short-circuit across the 71 to 86GHz frequency range. Figure 8 is a plot of the input impedance of a radial stub (green trace) and three values of MIM capacitor and ground (0.5pF, 1pF and 2pF). It can be seen that the radial stub provides a good short circuit at 80GHz whereas the MIM capacitors and vias all look inductive. Whilst it is possible to reduce the length of the λ/4 bias stub so that the capacitors are open circuit at the amplifier, the fact that they do not provide a good short-circuit at E-band means that the bias components (including the lower frequency stabilising components) can affect the in-band performance and reduce the gain slightly. Whilst this would not be a problem at lower mm-wave frequencies at E-band the available gain is marginal and every effort must be made to avoid reducing it. It was therefore decided to implement the demonstrator amplifier with radial stubs for the bias grounds. The resulting layout of the demonstrator amplifier is shown in Figure 9.

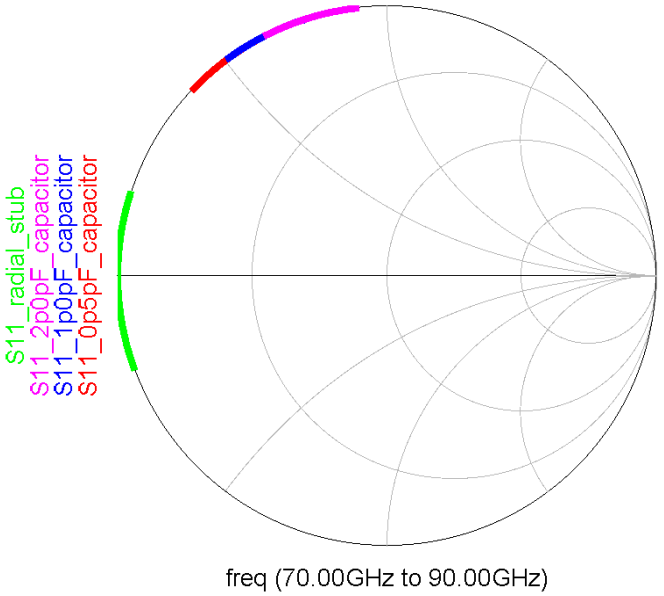

Figure 8: Input impedance of MIM capacitor and ground via compared to radial stub

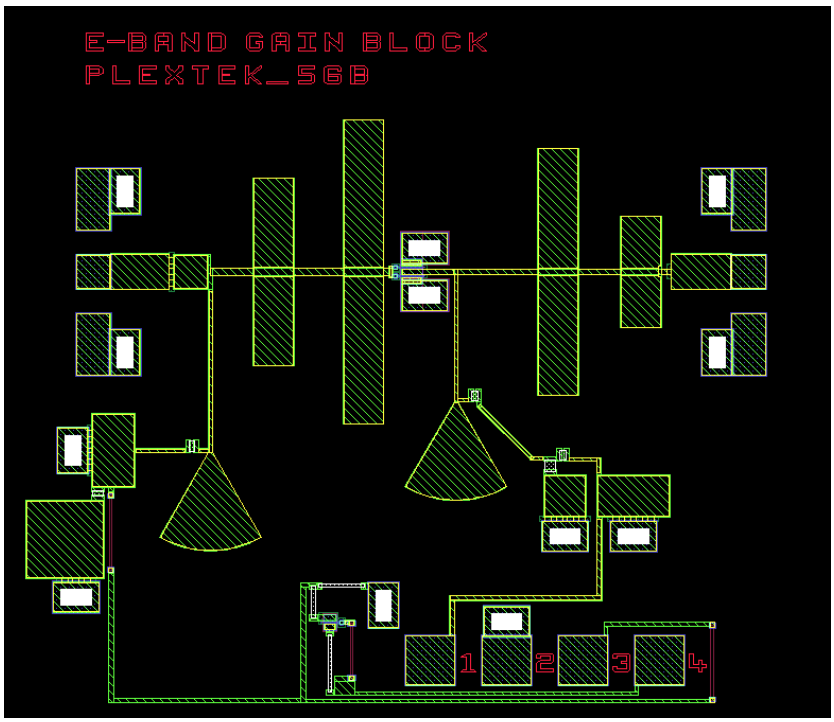

Figure 9: Layout of the E-band demonstrator amplifier

The demonstrator amplifier includes G-S-G pads for RFOW probing. An on-chip active bias network is included to generate the required Vgs from a fixed -3V supply. The use of active biasing provides improved unit to unit repeatability and reduced performance variation with temperature. Four DC pads are included, the +3V amplifier bias, the -3V supply to the active bias network, a pad to sample the gate voltage generated by the active bias network and a ground to allow convenient off-chip de-coupling during RFOW test.

The ideal components in the initial design were gradually replaced by practical component models. The final circuit simulated s-parameters are plotted in Figure 10. This simulation includes transmission line and MIM capacitor models and models for all tee and cross-junction discontinuities. A gain of around 5dB is achieved with terminal matches of around 10dB. The drain current was 11mA. Optimising over a narrower bandwidth would allow improved matches and slightly higher gain.

Although it is essential to EM simulate designs operating at such high frequencies the timescale for the tape out of the available mask set did not allow this and so all pre-fabrication simulation was based on circuit simulations only and no EM simulation was undertaken prior to tapeout.

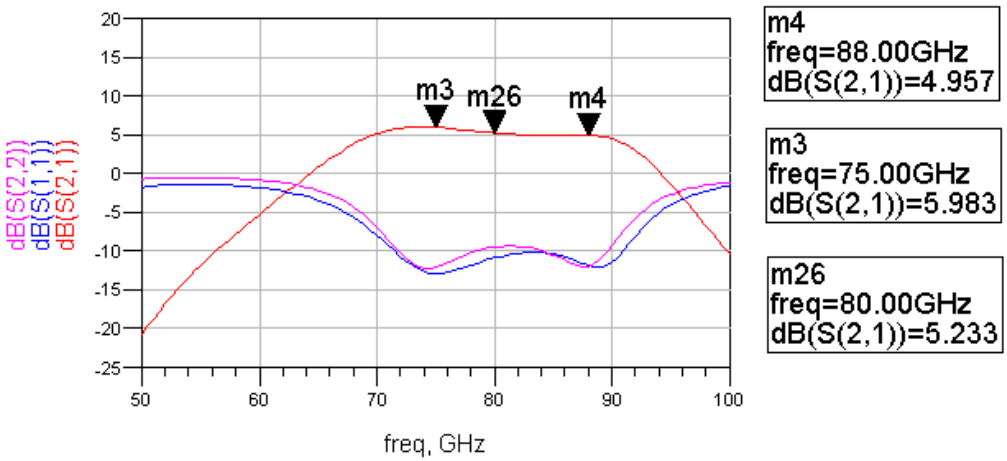

Figure 10: Simulated s-parameters of the single stage E-band amplifier (circuit simulation only, no EM)

The simulated NF of the demonstrator amplifier is shown in Figure 11 and is around 3.6dB at 71GHz rising to 4.3dB at 86GHz. The simulated 1dB gain compressed output power is plotted against frequency in Figure 12. At around 10dBm the power compression (and so linearity) of the amplifier is modest. It is believed that a design offering a little more power could be possible on this process but this is likely to be at the expense of gain. The maximum practical P-1dB from a single-chip E-band amplifier designed on this process is expected to be around 18dBm. This would utilise multiple power combined transistors. However, this approach provides diminishing returns as the combiner/matching networks further reduce the already modest gain.

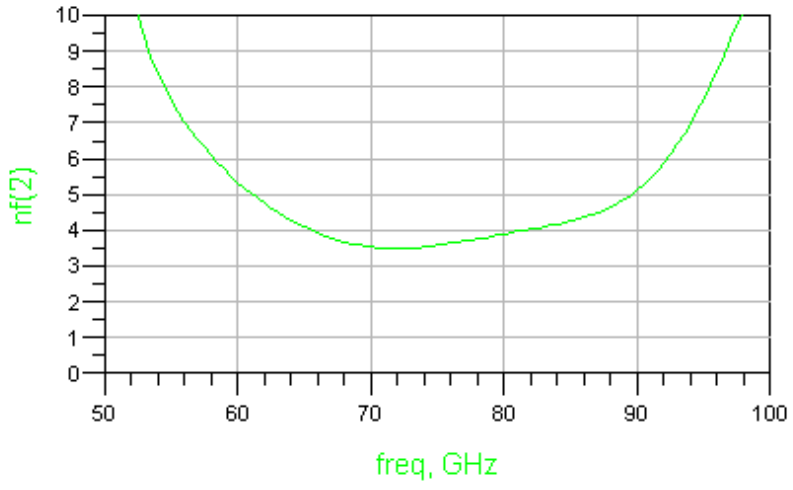

Figure 11: Simulated NF of the single stage E-band amplifier (circuit simulation only, no EM)

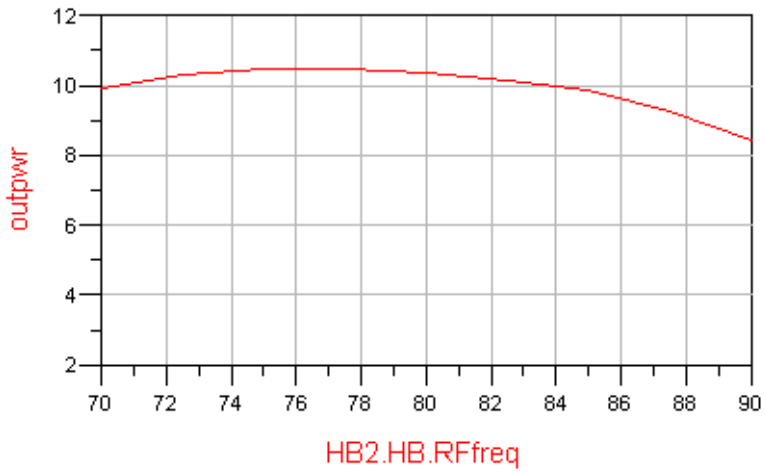

Figure 12: Simulated P-1dB of the single stage E-band amplifier (circuit simulation only, no EM)

4. Realisation and Measured Performance

The amplifier was fabricated on the PP15-20, 0.15µm gate length PHEMT process of WIN Semiconductor. It was realised as a sub-circuit within an array targeting a different application. As such it was only suitable for RFOW evaluation and is not available as a stand-alone die. A photograph of one of the E-band amplifiers is shown in Figure 13.

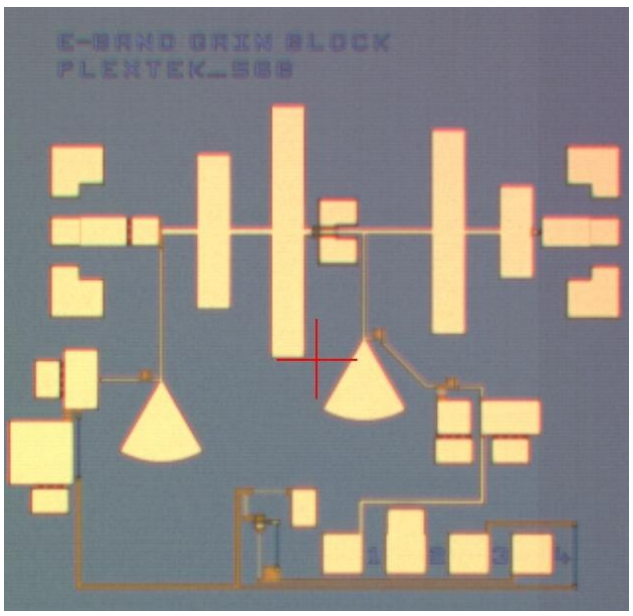

Figure 13: Photograph of the E-band amplifier

The s-parameters of the demonstrator amplifier have been measured and are plotted against the original circuit simulated performance in Figure 14 and Figure 15. As would be expected there is a modest reduction in gain and a drop in frequency of the overall response, particularly at the high end of the band. These effects can be adequately simulated and accounted for with detailed EM simulations as detailed in Section 5 below. Despite these differences the agreement between circuit simulated and measured performance is reasonable and indicates that the foundry models are adequate for design at E-band.

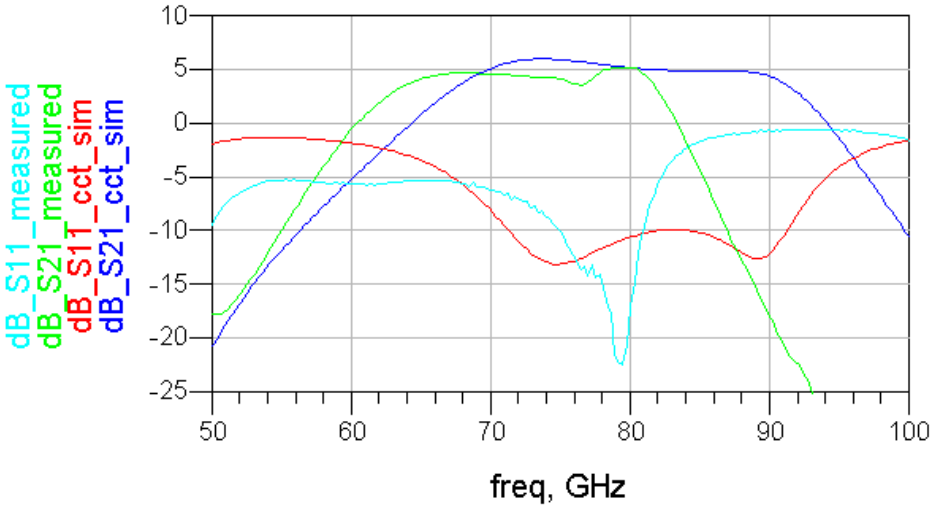

Figure 14: Measured versus original circuit simulated S21 and S11 for the single stage E-band amplifier

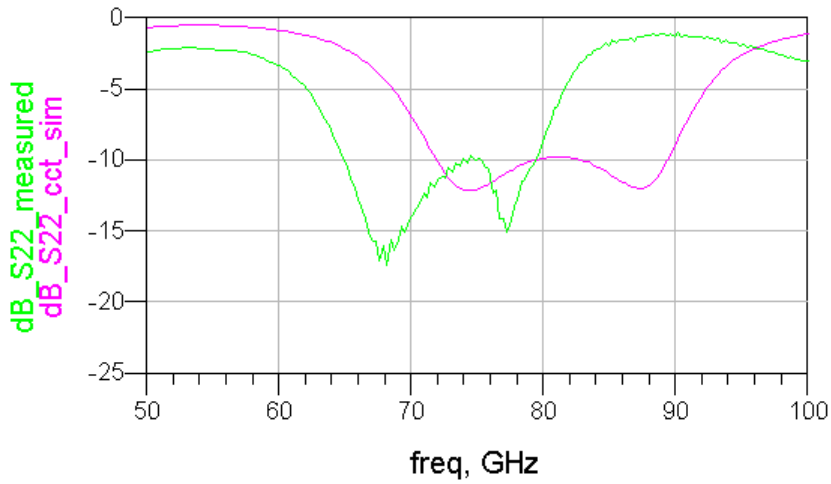

Figure 15: Measured versus original circuit simulated S22 for the single stage E-band amplifier

5. Post Realisation EM Simulated Performance

Following fabrication and measurement a detailed EM simulation of the design was undertaken. The EM simulated s-parameters of the demonstrator amplifier are plotted against the measured performance in Figure 16 and Figure 17. It can be seen, as would be expected, that the agreement with measured performance is considerably closer than for the circuit simulated performance. In particular the

prediction of high frequency gain roll-off is very close. This indicates that there is a viable route to designing and simulating E-band circuits.

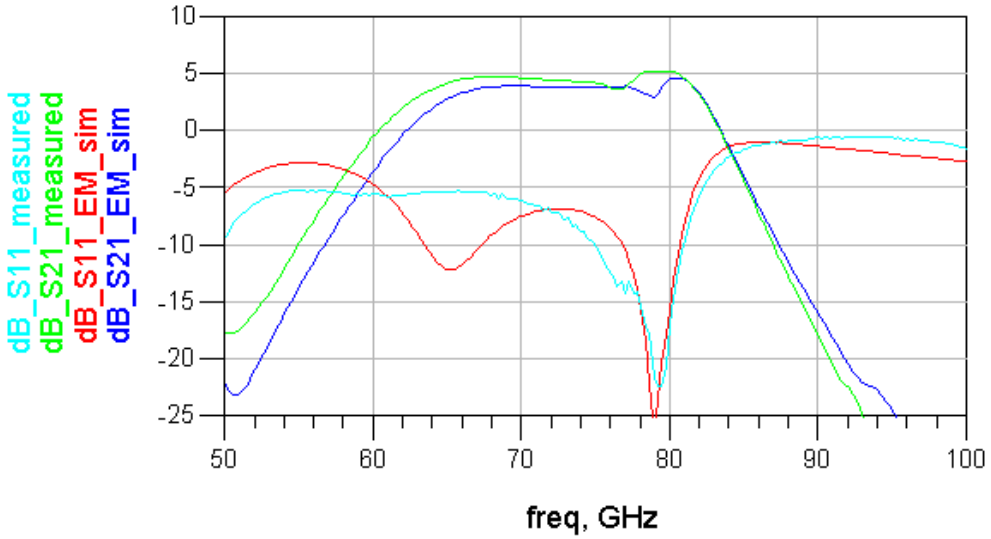

Figure 16: Measured versus original circuit simulated S21 and S11 for the single stage E-band amplifier

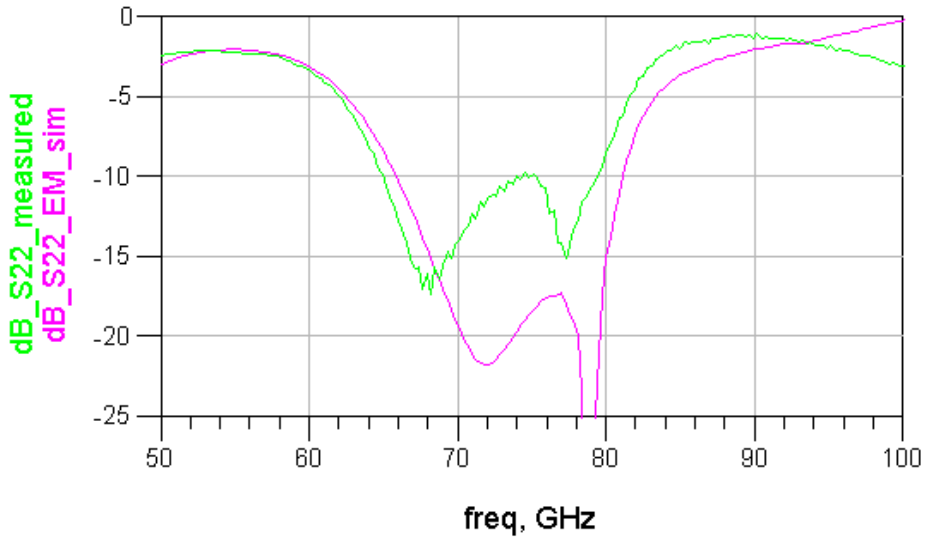

Figure 17: Measured versus original circuit simulated S22 for the single stage E-band amplifier

6. Summary and Conclusions

This paper has described the challenges of implementing E-band circuit functions using commercially available MMIC processes. It has considered process selection, effective design approaches and has presented the measured versus modelled performance of a demonstrator single-stage E-band amplifier realised on WIN Semiconductors 0.15µm gate length power PHEMT process (PP15-20). EM simulation of the layout was able to provide a good correlation between modelled and measured performance and offers a viable route to the realisation of multi-function E-band MMICs.