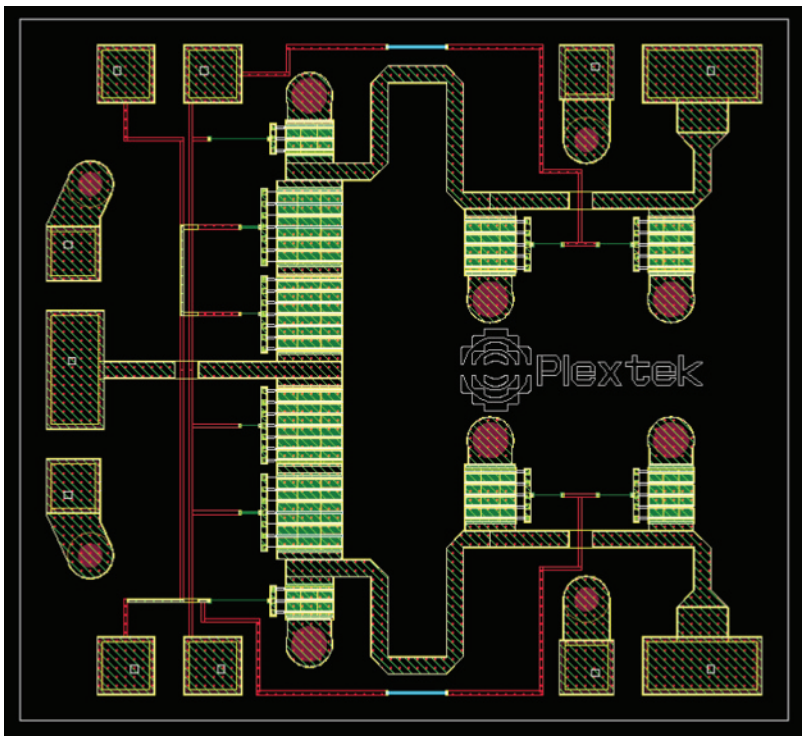
Case Study

DC to 20GHz High Linearity GaN SPDT Switch MMIC

GaN technology is now widely adopted for high power microwave amplifiers. The high breakdown voltage of the transistors is key to their ability to provide high power amplification and it also means they can be used to realise very high linearity RF and microwave switches. This case study describes the design and implementation of a DC to 20GHz Single Pole Double Throw (SPDT) GaN MMIC switch. It offers an IP3 of 62dBm with an insertion loss of just 0.75dB at 1GHz rising to 1.3dB at 20GHz. Isolation is over 45dB and the die size is just 1.6mm^2.



DC-20GHz SPDT GaN Switch Layout

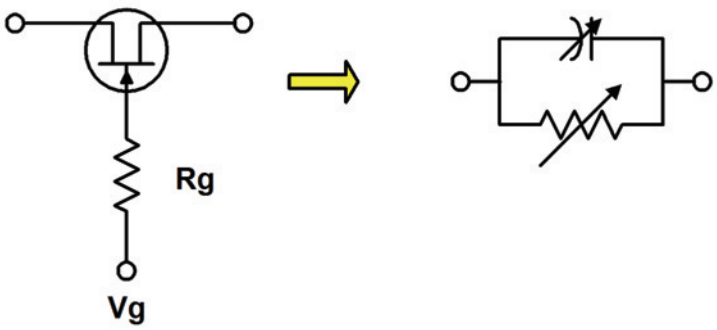
GaN transistors as switches

GaN transistors can easily be configured to perform an RF switching function. Their suitability for switch realisation stems from the fact that the drain-source resistance behaves as a voltage variable resistor, the resistance being set by the gate-source voltage. When used as a switch, the transistor is operated with the drain and source at zero volts DC. The RF signal path is drain to source and the gate is the control terminal.

In the region of Vds=0V, the Vds/Ids characteristic approximates a resistance (Ids $\propto$Vds). For Vgs=0V this is a low drain-source resistance (the transistor is on) and for Vgs below pinch-off (typically around -3 to -5V for GaN processes) it is a high drain-source resistance. This gives rise to the simple approximate equivalent circuit, shown below. A gate resistor (Rg) is included as a simple and effective means of providing isolation between the RF signal path and control port, a value of several kΩ is typically used. The parasitic capacitance, in parallel with the resistor, limits the isolation that the transistor can provide, and tolerating this is one of the key challenges in the design process.

Plextek RF Integration Plextek Ltd., London Road, Great Chesterford, Essex CB10 1NY UK

T: +44 (0) 1799 533200 **E:** enquiries@plextekrfi.com **W:** www.plextekrfi.com



Simplified model of a GaN transistor as an RF switch

The layout of GaN transistors for optimum performance as an RF switch is slightly different to the layout of amplifying transistors. The GaN process itself is the same and switch transistors and amplifying transistors can be realised on the same die. The main differences between switch transistors and amplifying transistors are:

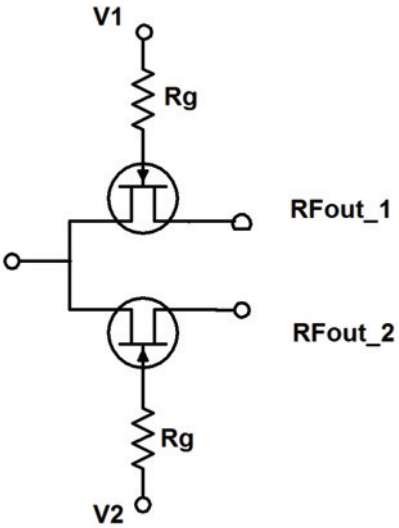
- The amplifying transistors include integral grounded sources (connected to the back side of the die using through substrate vias)
- The gate finger pitch of the amplifying transistors is greater than that of the switch transistors. This improves the thermal performance (ability to dissipate heat without getting too hot) but does increase the die area occupied by the transistor. As a switch transistor normally dissipates much less power than an amplifying transistor it can tolerate a smaller gate pitch.
- Switch transistors feature a gate placed centrally between the source and drain. This symmetric structure results in maximum RF power handling, with Vds=0V and in the off-state, for a gate bias voltage centred between the breakdown and pinch-off voltages for the process.
- Switch transistors do not include a source coupled field plate. This improves the RF performance of the switch (reducing parasitic capacitances) but reduces the breakdown voltage. Although the breakdown voltage is reduced it is still impressively high and control voltages in the range -25V to -40V are typically used.

The basic approach for designing RF GaN switches is straightforward. The simplest SPDT switch uses a single series mounted transistor in each arm, as depicted below. Control voltages V1 and V2 are complimentary (V1 being "low" when V2 is "high" and vice-versa). This topology can offer low loss but limited isolation, which degrades further with increasing frequency. This degradation in isolation is caused by the parasitic drain-source capacitance shown in the simplified equivalent circuit above. The choice of transistor size (total gate width) largely determines the performance of this simple SPDT. Increasing the total gate width of the transistor would reduce the on-case insertion loss but would also degrade the isolation. This topology is only suitable for use at relatively low RF frequencies and more complex topologies must be adopted to extend the switch performance up into the microwave frequency range.

Design approach for the DC to 20GHz switch

The simplest way to extend the upper operating frequency of the SPDT shown below is to add a shunt device to the output of each arm. These operate under complimentary control to the corresponding series device and extend the practical upper operating frequency. However, whilst this approach does extend the upper operating frequency it does not come close to allowing useful performance to 20GHz. For such wide bandwidths as this a distributed architecture is most appropriate, which was the approach adopted in this design. The circuit schematic of the DC-20GHz SPDT is depicted on the following page.

The key to extending the upper operating frequency of the switch is to embed the shunt transistors (Q2, Q3 and Q4) in a low pass filter structure. When these transistors are pinched-off their shunt capacitance combines with the series inductors (L2, L3 and L4) to form a low pass filter with low insertion loss over the required operating band.



Simple series only SPDT

When the shunt transistors are on (Vgs = 0V) their low resistance transforms the low pass filter into a high value attenuator providing isolation for the off-state arm. Complimentary control voltages V1 and V2 (in this design 0V/-40V) set each arm of the switch into opposite states (if the top arm is the on-path the bottom arm will be the off-path).

The series transistors Q1 are pinched-off when the shunt transistors in the corresponding arm are set to their low resistance state (i.e. high RF path loss). The off-state series transistors transform the low impedance at Q2 to a high impedance at the input. At the same time the other pair of series transistors are biased at Vgs = 0V and provide a low impedance through path. The following shunt transistors are pinched-off and the switch arm behaves as a low pass filter. Thus the overall switch has one low loss on-path and one high isolation off-path.

The use of two series transistors Q1, rather than a single transistor, is related to providing improved linearity as discussed below.

Small Signal Performance

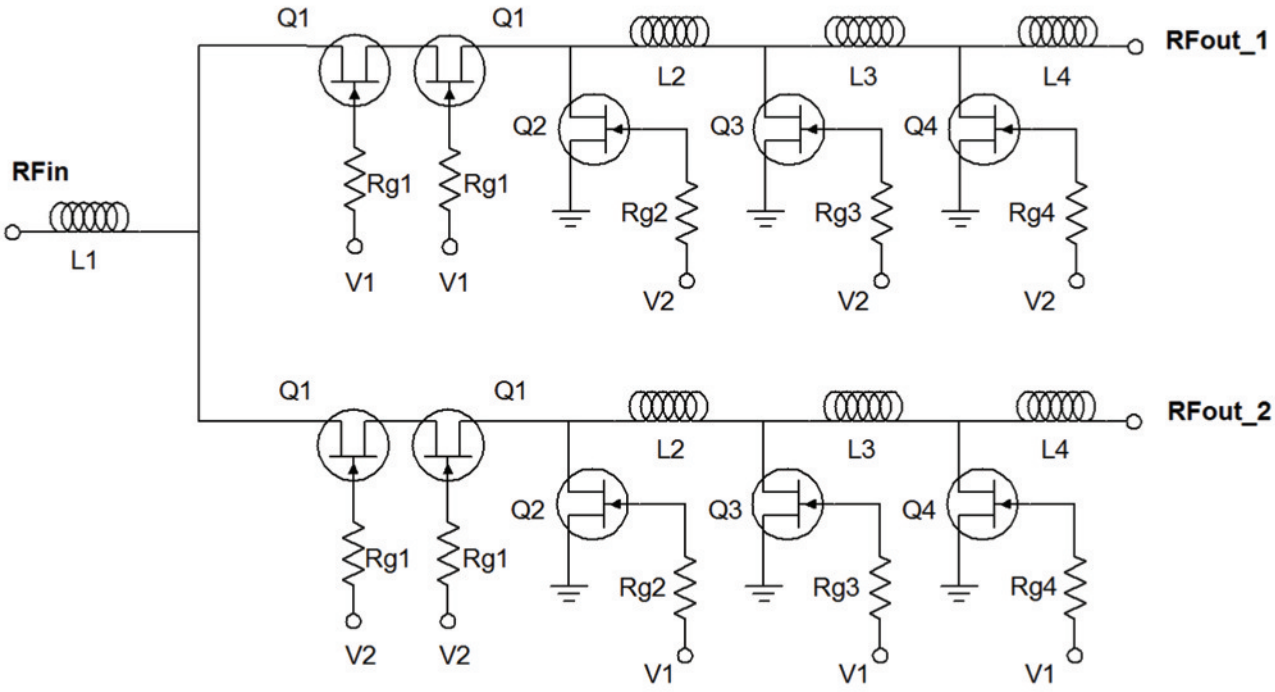
Small signal performance is shown in the two plots below. Insertion loss of the on-state path is just 0.75dB at 1GHz rising gently with frequency but still less than 1.3dB at 20GHz. Input and output return losses are better than 18dB to 20GHz. The isolation of the off-state path is higher than 45dB to 20GHz.

Power Handling and Linearity

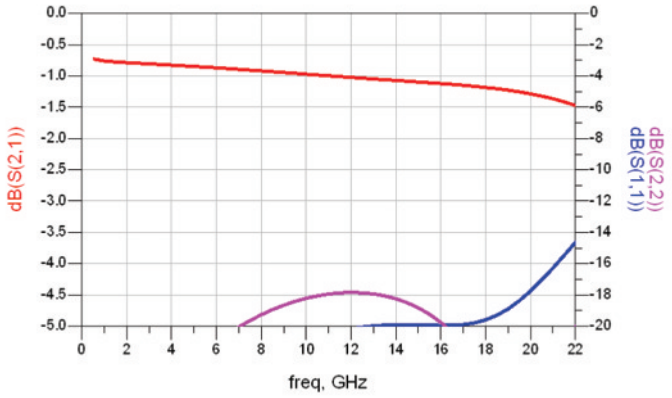
Transistor large signal models are normally optimised to simulate the performance of the transistor as an amplifier and are often not well suited to accurately modelling switch compression and linearity.

Fortunately it is possible to estimate the power handling performance with a reasonable degree of accuracy. The peak power handling of the switch MMIC is determined by the ability of off-state transistors to handle the associated RF voltages and the ability of the on-state transistors to handle the associated RF currents. Power handling of both the on-state and off-state devices must be considered in order to determine the power handling capabilities of the entire switch.

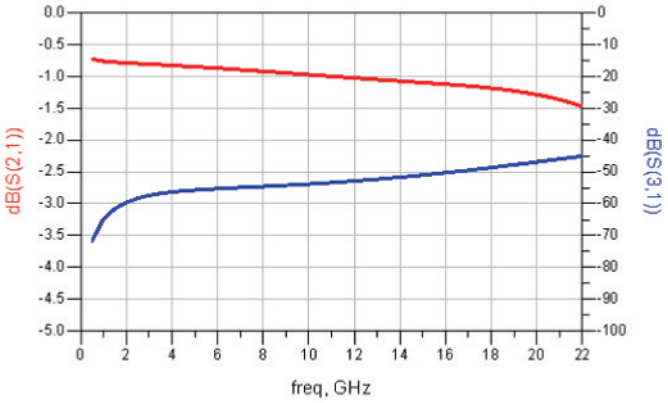
For the on-state devices the peak RF current flowing through the series transistors dominates. The larger the series transistor the higher its current handling capability and the higher the RF power level it can pass before compression.



Schematic of the SPDT GaN switch



Insertion loss and return losses of the GaN SPDT



Insertion loss and isolation of the GaN SPDT

Generally speaking the higher the upper operating frequency of a switch the smaller the series devices that need to be used. Viewed simplistically the use of two series devices in cascade allows the size of the transistor to be doubled whilst maintaining the same insertion loss and isolation. This means an increase in power handling of 6dB compared to using a single series transistor. In reality the additional parasitics associated with a larger transistor mean that the performance at microwave frequencies actually degrades slightly for a cascade of two transistors of double the size and there is a trade-off between small signal and large signal performance. For the design presented here the estimated 1dB compression point of the series transistors is 42dBm and the IP3 point around 62dBm.

For the off-state devices compression occurs when the RF voltage swing causes the gate-drain breakdown voltage to be exceeded on the positive half cycle or when it moves the transistor out of pinch-off on the negative half cycle.

The high breakdown voltage of the GaN transistors allows a control voltage of -40V to be used. The effective P-1dB point of the off-state transistors is estimated at around 48dBm, which means that the compression performance of the on-state devices dominates.

The compression and linearity figures above are valid for frequencies above around 100MHz. The compression performance of HEMT switch transistors degrades at very low frequencies. The is a well known phenomenon, which is described in more detail in a paper entitled "The Design of Integrated Switches and Phase Shifters" available for download from the Plextek RF Integration website:

http://www.plextekrfi.com/publications/publications-from-plextek-rfi

Consideration must also be given to the maximum power dissipation that the switch can tolerate. It is possible to design GaN switches with very high theoretical P-1dB points that would dissipate a damaging amount of power before the P-1dB point was actually reached.

Summary

GaN transistors can be used to realise RF and microwave switches with very high power handling capabilities. The design presented here is a Single Pole Double Throw (SPDT) switch realised on a 0.25µm gate length GaN on SiC process. The switch covers DC to 20GHz with an insertion loss of just 0.75dB at 1GHz rising to 1.3dB at 20GHz. Isolation is over 45dB and IP3 62dBm. The overall die size is 1.6mm^2.