Low Power Techniques for Silicon RF ICs

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1 Introduction

Silicon RF ICs provide functions suitable for processing of a signal being received or of a signal to be transmitted. These include RF amplification, signal generation, modulation and frequency conversion. The benefits of integration include reduced component count, control of parasitics, definition of architecture breakdown and signal levels, shrinkage of area, improved product yield, potentially reduced cost, improved signal matching and interference immunity

Low power techniques are important for a number of applications including battery powered radio systems such as cellular and cordless products, radio pagers and remote meter readers where extending the time between battery recharge/change is a dominant design goal. For example, second generation pagers are required to operate for up to 1 year on one 'AA' cell and meter readers are expected to operate for 10 years without battery recharge or battery change.

To reduce power consumption in an application it is necessary to look at all levels of design and all areas of design. Although the focus of this talk is on low power techniques for silicon RF ICs it is of course necessary to consider the other areas of the design where power reduction techniques would apply such as: How is low frequency processing performed? – in the analogue or digital domain; what level of digital activity does the application require? – the lower the switching rate of logic gates, the lower the power consumed – and so on.

Techniques to minimise power consumption can be controlled at four stages in an application: the system level, the architecture level, at the circuit level and at the technology level. It is unlikely for an individual designer to have control at all of these levels: for instance the system operation of the application may already have been designed – possibly at international level, or the technology choice for the application may be limited by product volume and cost targets.

In this paper, we will briefly cover opportunities to minimise power at the system, architecture and technology level, and look in more detail at circuit level techniques that have been used in low power silicon RF ICs.

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2 Techniques to minimise power in Silicon RF ICs

2.1 System Level

By the 'system' level of a design, we are referring to the protocols by which the application operates. For example, in a cellular system, the protocols have been designed by international groups resulting in air interface definitions for GSM / IS95 / DCS-1800. Similarly pager systems are defined by the POCSAG, ERMES and FLEX air interface definitions. If protocols are designed with power saving in mind, then the designers will have considered aspects such as how much data and how frequently must data be transmitted, and set transmission and reception periods to allow for battery saving.

To achieve a power saving, arrangements are made to turn off all non-essential circuits when they are not required. For example, remote meters transmit a small amount of information, typically the meter address and reading, infrequently. As a consequence advantage is made of this very low duty cycle to place the unit into standby mode for those times it is not transmitting.

If large amounts of data are transmitted regularly, then a synchronised transmission system may be designed so you know when to turn on to receive information that may be for you. For example radio paging systems are designed to extend battery life by having regular time slots when a message could be sent to a unit. The unit turns on for the start of those known time slots to look for a transmission and turns off immediately afterwards. Further savings are made when a transmission is detected but the address, when decoded, is found to be for another unit; under these circumstances, the pager would be designed to turn off early as it does not need to stay on to decode a message intended for another unit.

An important aspect of power saving techniques is that a breakdown will show that battery lifetime is often dominated by the unit's power consumption in standby mode[1], so minimisation of power in this mode becomes a major design goal for extended battery life. Also important is the need to ensure the turn-on settling time of the unit is short with respect to the 'on-period'.

Choice of transmission frequency will affect consumption – for example applications operating in the gigahertz range will consume more power than their counterparts operating at say 200MHz.

Efficiency in transmission is another area where careful system choice can lead to power savings. If a constant envelope scheme is chosen as the method of data modulation, then non-linear power amplifier techniques can be applied with their considerable advantage in efficiency over the linear configurations needed for non-constant envelope schemes[2].

2.2 Architecture Level

By the 'architecture' level of design, we are referring to the specific method of physically realising the application. For example, a superhet receiver architecture will be structured to include one or more intermediate frequencies before demodulation and comprise off-chip band-pass crystal or ceramic filters for selectivity.

Architecture innovation is a technique that can reduce product complexity and along with that, power consumption[3]. Here are a few examples:

- Kasperkovitz[4] produced, in the early 80's, a highly integrated FM radio receiver with reduced size and power dissipation by eliminating many off-chip passive components. Here the receiver used a novel 70kHz IF allowing selectivity to be integrated on-chip.
- Vance[5] developed a zero IF receiver and applied it to paging applications. The advantages included channel selectivity by low-pass audio frequency filters and avoiding the need for image filters or crystal channel filters. The zero-IF approach with its characteristic 'hole-in-the-middle' in-band spectrum gave an excellent match to the modulation characteristic of paging transmissions.
- Philips[6] took the zero-IF concept and fully integrated all active devices onto a single bipolar IC giving power, size and cost advantages over superhet competitor products.

Architecture simplification is another technique that can reduce power consumption. Here we mean studying the architecture to look for ways in which the functional blocks can be rationalised. For example, Is it possible to simplify to use one oscillator to generate all frequency sources?

Power minimisation per function requires the designer to consider the specific needs of each stage of the architecture and ensure it is designed with the minimum power to realise the required performance, be it signal-to-noise, carrier-to-phase noise, 3rd order intercept etc. Perform processing at low frequencies to minimise power, not forgetting that capacitors increase the power necessary to achieve a given BW

Careful selection of battery sources for the application is essential for power minimisation and the following questions need consideration:

- What is the lifetime of the application?
  - Products operating for 10 years without change or recharge require batteries with very low self-leakage in addition to the capacity to supply the charge over that time.
- Is the product expected to operate in all parts of the world?
  - 'AA' cells are available world-wide, but others such as lithium button cells have a more restrictive outlet.
- Is the application to be driven directly from the battery?
  - Aim to match the battery minimum terminal voltage with the minimum voltage required for the circuit structures.
  - Aim to rationalise the circuit structures to operate from – if possible – one voltage rail.
  - Ensure the battery characteristic with temperature, state of charge and load demand is sufficient.
- Is the application to be driven via a DC-DC convertor and/or regulator?
  - What is the efficiency of the convertor
  - How much power is lost in the convertor / regulator

The location of the analogue-digital interface has an impact on consumption. It requires the designer to ask at what point in the architecture does it become more efficient to use an analogue or a digital realisation of a function? What level of digital activity does the application require? And so on.

2.3 Technology level

By the technology level, we are referring to the technology choices on which the whole architecture is based. These include the choice of IC process for the realisation of the application together with choice of component and battery technology.

The majority of IC processes used in RF applications use planar fabrication techniques, starting with a silicon wafer and using sequences of photo-masking, diffusion, epitaxial growth, oxidation and ion implantation to build transistors, resistors and capacitors. One process will differ from the next in terms defined by mask resolution, doping concentrations and profiles, diffusion and implantation depths, epitaxial and oxide thickness; these parameters set the numerous constants that are used to characterise the simulation models of the components of the process. By careful selection of the process, a designer is able to optimise the performance of the circuitry against power consumed.

More exotic RF processes specifically aim to reduce parasitic capacitance – for example processes exist that invert the finished wafer and bond it onto a second substrate. The silicon wafer is then etched back to remove the (first) silicon substrate and thereby remove all parasitic capacitance to that substrate, with the effect of allowing the desired frequency response to be obtained at a lower consumption.

Improvements in component technology has led to improved circuit performance over the years: Q's of surface mount inductors and capacitors are much higher now than when they first became available and these improvements have led to higher circuit efficiency

Improvements in battery technology over time have led to increases in charge capacity, and decreases in self-leakage, per unit volume.

2.4 Circuit level

By the 'circuit' level of design, we are referring to the detailed construction of components and stages comprising the architecture. Here we will look at a number of specific functions found in silicon RF ICs. The optimum solution to a particular problem may be to realise the design as fully integrated, wholly discrete or as a combination of both discrete and integrated circuit techniques. In the following we will look at functions that fall into the latter category.

2.4.1 Single ended amplifiers

These are used off-chip for simple functions where performance is premium. Here the designer is not limited to the characteristics of one IC process and is able to benefit from the simpler packaging and lower losses of a discrete device. The trade-off comes in the extra area that the discrete solution occupies and in the level of complexity that the designer is prepared to accept. For example, if a low noise amplifier is to include an AGC system, then allowance for PIN diodes and control line decoupling will be necessary in addition to the amplifier support circuitry. When a design target includes size minimisation, it may be necessary to realise such functions on-chip.

Techniques to minimise power include operating the stage from a low voltage rail and with a forward biased collector-base junction to take the active device as close as possible, but not into, saturation. In addition, using the highest possible load impedance for a particular gain will allow the transconductor bias current to be minimised. Realisation of the load will be application dependent; for broadband applications, the bandwidth will be limited by the stray capacitance and this in turn will determine the load impedance that can be realised. For narrow band applications, higher impedances are possible as stray capacitance can be reduced by resonance with an inductive element. See figure 2.4.1.1

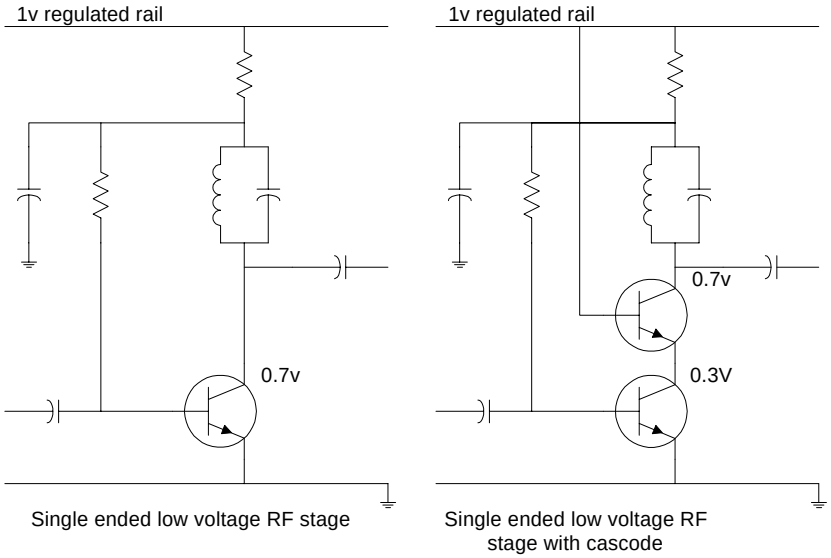

Figure 2.4.1.1 Low power single ended structures

Biasing techniques for such approaches need to be carefully applied. The diode-connected approach is well suited as it allows the emitter to be directly grounded, however a regulated rail needs to be provided, often with a voltage temperature coefficient.

2.4.2 Differential amplifier

These are realised on-chip for a number of applications including amplifiers for small signals and limiters and frequency multipliers for large signals. Their balanced nature minimises common mode interference and allows them to be directly connected to previous stages to simplify biasing needs. As with single ended devices, similar techniques to minimise power can be adopted:

- Maximise load impedance to minimise stage current for a given gain
    - Off-chip LC type: realised off-chip offer highest impedance, penalty is pin-out but matching to following stages is possible, see figure 2.4.2.1
    - On chip LC type: possible at >1GHz, but Q_{load} poor and large chip area for L
    - On-chip resistive: offer small size but supply current dissipated in resistor. On-chip strays are much smaller than those off-chip. Difficulties in interstage matching.

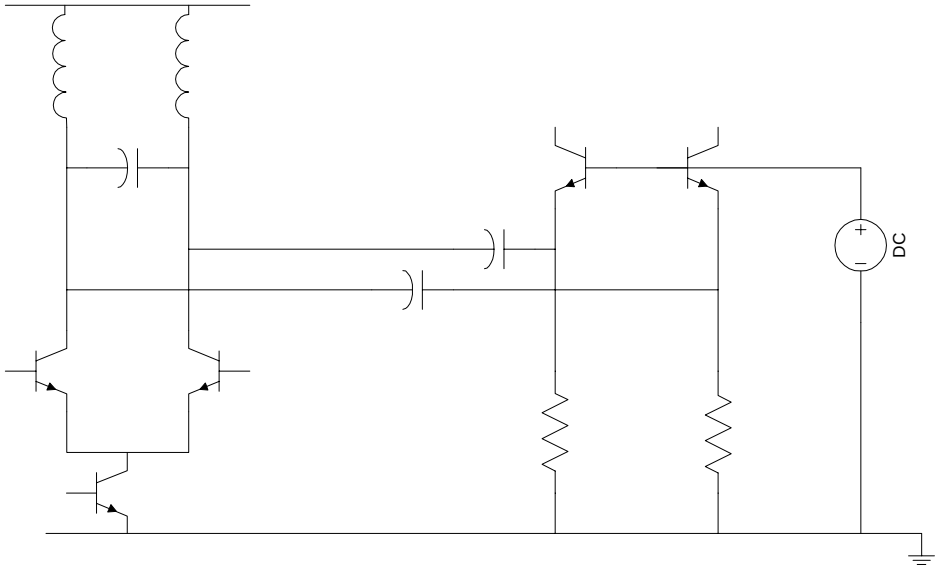

Figure 2.4.2.1 LC interstage match

- Operate with base-collector junction forward biased
- Minimise stray capacitance to avoid unnecessary signal leakage into substrate from (see figure 2.4.2.2):
    - transistor collector, (reducing device size may not be possible as it may degrade other parameters at the same time so introduce a small size cascode if there's the headroom)
    - resistor parasitic capacitance (minimise dimensions)
    - load capacitance (minimise size of input device)
    - interconnect

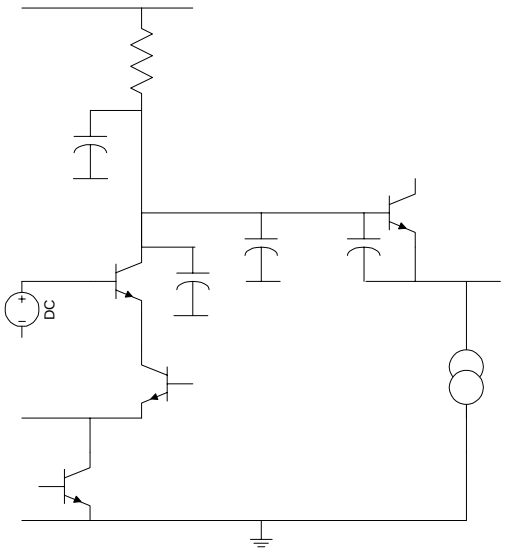

Figure 2.4.2.2 Parasitic capacitance

2.4.3 Dividers

These are realised on-chip. They are used in frequency synthesisers and to provide quadrature drives for up and down conversion and modulation. Usually the input is differential and requires a 150mV pk signal swing to fully route the divider current. Master-slave types (Figure 2.4.3.1) operate down to DC and quadrature divide by two accuracy is dependent on the even order harmonic distortion of the input signal; an uneven M-S ratio leads to divergence from the 90 degree phase difference ideal.

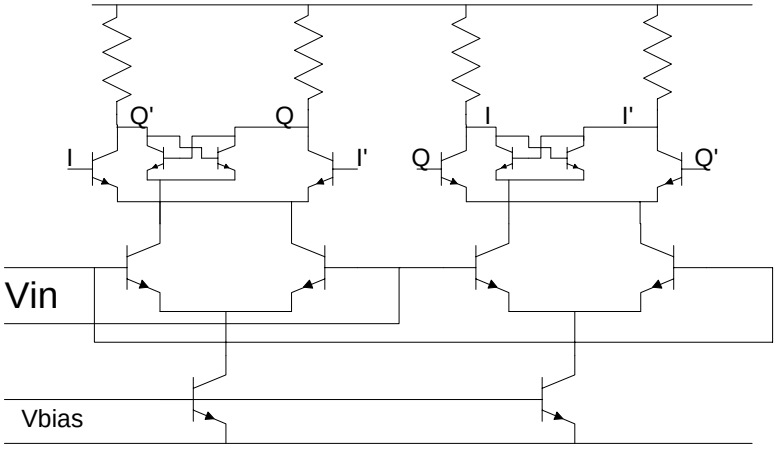

Figure 2.4.3.1 Master slave quadrature divide-by-two

Travelling wave types[7] (Figure 2.4.3.2) minimise the number of components and thus strays to realise the function and consequently operate at the highest frequency for a particular current and technology. They operate over a limited range of frequencies.

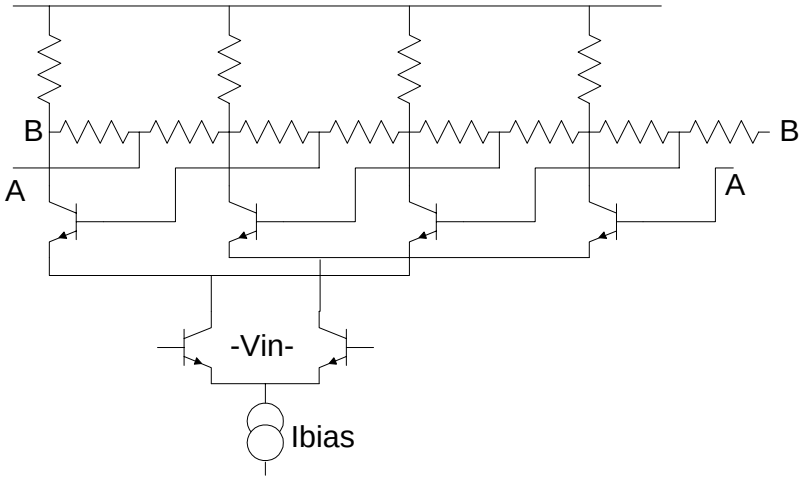

Figure 2.4.3.2 Travelling wave divider

Again further power reduction techniques include:

- Maximising load impedance to minimise stage current
- Operate with base-collector junction forward biased
- Minimise stray capacitance by reducing device size, interconnect and load dimensions.

2.4.4 Mixers

These are used on chip to provide quadrature up-conversion, modulation and down-conversion functions; and the Gilbert cell structure[8] is almost universal; figure 2.4.4.1 shows two common variants often seen. Note that the three layer stack of devices in each mixer require a voltage rail that is greater than 1V to obtain an adequate performance.

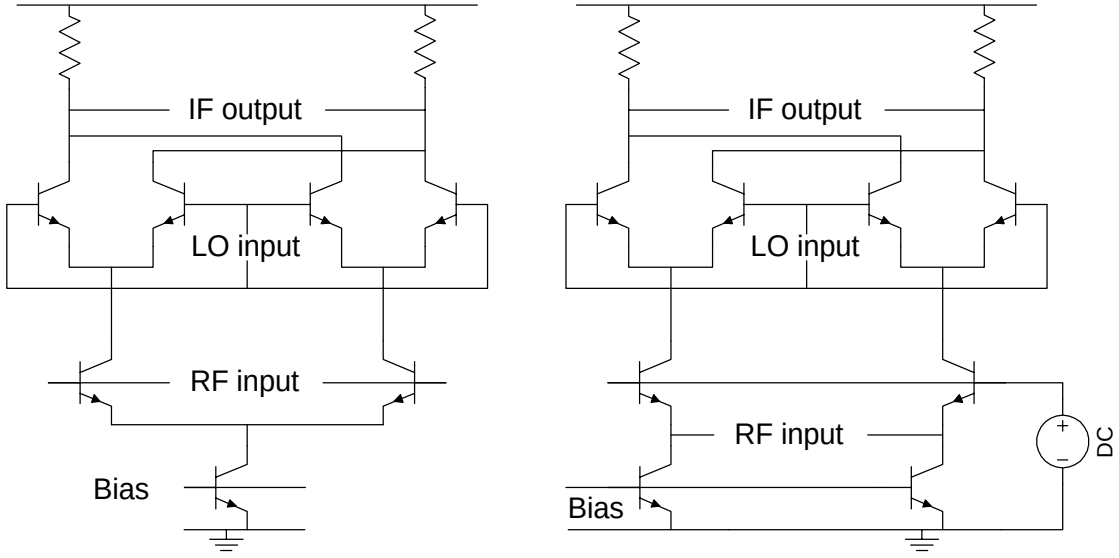

Figure 2.4.4.1 Emitter coupled and common base versions of the Gilbert cell mixer

Figure 2.4.4.2 shows an interesting variant that has been applied in products[9]: the lower RF input stage has been removed to achieve a mixer that operates on a 1V supply.

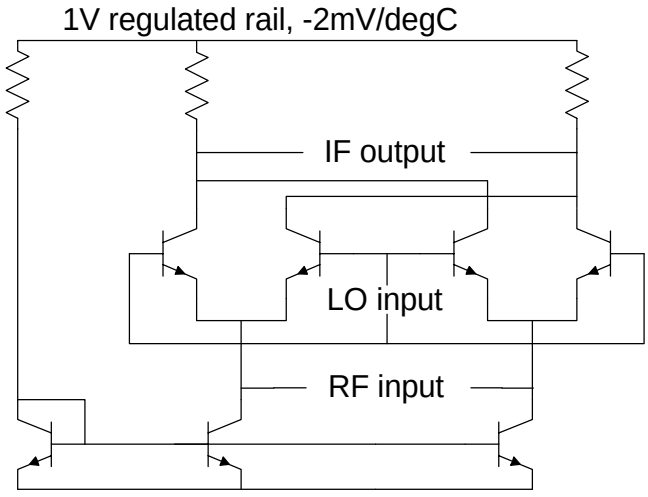

Figure 2.4.4.2 Low voltage double balanced mixer

2.4.5 Off-chip supplies

Sometimes it is necessary to provide supplies to power off-chip active devices. The example of a single ended device (section 2.4.1) required a 1V regulated rail and this is often provided by support circuitry on the IC. Figure 2.4.5.1 shows one example - an off-chip pnp being driven by an on chip regulator comprising op amp and voltage reference. If the regulated line is required to have a voltage variation with temperature, then this characteristic is built in to the on-chip regulator. The advantage of using a pnp – from the low power point of view - is that it allows the battery to continue to supply the load to within 50 to 100mV of the regulated output. Again the technique is to operate towards saturation.

It would be advantageous if the regulated pnp were integrated; the feasibility of this is dependent on the features of the IC process. High Ft Bipolar and BiCMOS processes used in wireless applications usually use lateral pnp devices. Such devices consume a considerable area per unit of emitter current and it is often uneconomic to allow for this on the silicon die.

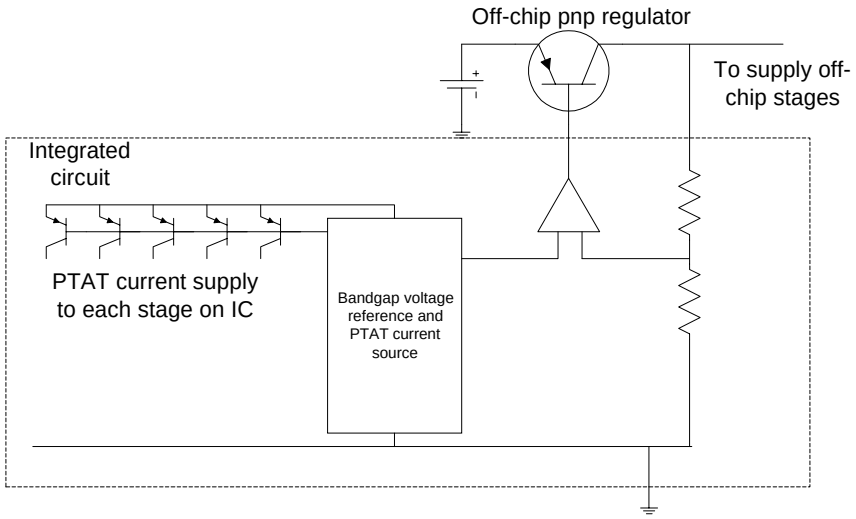

Figure 2.4.5.1 Chip biasing

2.4.6 On-chip biasing

The bias sources for all stages in an IC are often generated in a specific housekeeping block. Bias, in the form of currents or voltages are then routed to each stage or group of stages. Figure 2.4.5.1 shows an example where pnp current sources produce the bias for five different stages. In this example, the bias current has a characteristic that is proportional to absolute temperature: PTAT. This approach is often used where the transconductance of a stage is to be invariant with temperature; a bipolar transconductance is given by:

$$G_m = \frac{qI_c}{kT}$$

Individual stages are often biased by a current source connected to the emitters of a differential stage. In figure 2.4.6.1 we see the case where a number of stages are biased together from one common bias rail. The bias source size must be chosen with care. It is important to maintain high impedance on the virtual ground point of a differential stage to maintain good rejection of common mode signals, so minimising the size of the bias transistor collector will minimise the collector-substrate capacitor at this point. However, there is a trade-off as minimising the bias transistor size will lead to less accuracy in match with the reference transistor and a larger spread in bias current for the stage.

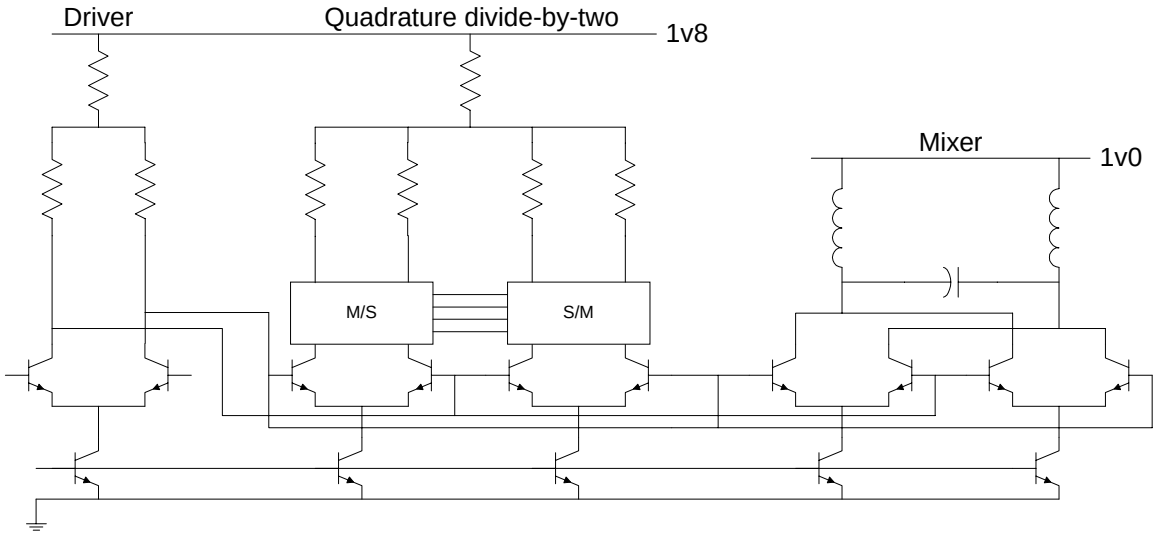

Figure 2.4.6.1 Integrated local oscillator chain

The same figure also illustrates the example of direct biasing of signal inputs from previous stages, removing the need for separate base bias power and decoupling.

3 Conclusions

This paper has reviewed techniques by which power consumption may be minimised and shown that this must be done globally to achieve maximum effect; we have looked at the four stages of a design that engineers can control: the system, architecture, circuit and technology levels.

We have also focussed on specific circuit techniques to minimise consumption that can be found on low power silicon RF ICs, and these include:

- Operation of active devices near to saturation.
- Minimisation of parasitic capacitance.
- Minimisation of components per function.
- Maximisation of load impedance.
- Direct biasing of stage(s) from a preceding stage.

4 References

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