An LTCC Based Differential Microwave DRO Module

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Abstract

Low Temperature Co-fired Ceramic (LTCC) technology is a multi-layer ceramic process that is well suited to the realisation of low cost, high performance RF and microwave components. This paper describes the design, fabrication and evaluation of a 21.3GHz differential Dielectric Resonator Oscillator (DRO) module fabricated in LTCC. It has a measured output power of +3dBm and an amplitude imbalance between the output ports of < 0.2dB. The measured phase noise is –102dBc/Hz at 100kHz offset from carrier. The module was the prototype of a commercial product that is now under development. The commercial product will also include a small voltage tuning range to allow phase locking of the DRO for applications such as clock generation in 40Gb/s optical transceivers.

Overview of LTCC Technology

Low Temperature Co-fired Ceramic (LTCC) technology is a low cost process for fabricating multi-layer ceramic structures. A wide range of materials and processes are available. The DRO module described here was fabricated by C-MAC MicroTechnology using Ferro A6 material. An overview of the fabrication process is given below:

- Ceramic layers are tape-cast in their pre-fired “green-state”
- The tape is cut to size and registration holes and via holes are punched into the different tape layers
- Via holes are filled
- Conductor patterns are defined on each layer using thick film processing
- Printed resistors are defined on any required layers using thick film processing
- The different layers are inspected, registered, laminated and then co-fired at around 850°C
- Circuits are DC tested and tiles sawn to separate the different circuits

The thick film processing used throughout allows line widths/gaps down to 100μm to be realised. Although the above description of the LTCC process may sound similar to that used to fabricate conventional multi-layer circuit boards using laminate materials such as FR4, LTCC has a number of advantages:

- Lower loss dielectric (lower tanδ)
- Better controlled dielectric properties (ε_r, tanδ and thickness)
- It is well suited to producing modules in low-cost SMT packages, including BGA topologies
- LTCC processes can produce modules, which are well suited to incorporating bare die as cavities and integral heat-sinks can be easily realised
- It is possible to include integrated, printed resistors and capacitors

Whilst the advantages of lower tanδ and better control of dielectric properties can also be achieved with traditional thick film ceramic processes, LTCC can also offer a number of important advantages over these processes:

- Layers are produced in parallel resulting in reduced costs and increased yields
- There is only a single firing operation (taking around 4 hours) so reducing production time and cost
- Each layer can be inspected prior to stacking, which improves yield
- The multiple layer structure allows the realisation of innovative printed structures such as baluns and filters and facilitates miniaturisation

Although LTCC is very well suited to realising RF and microwave components, many materials and processes are poorly characterised at RF frequencies. This work used data obtained from a characterisation programme previously carried out by Plextek [1]. An example of this characterisation data is shown in Figure 1, which is a plot of the ε_r versus frequency for Ferro A6 material. This was measured on a range of ring resonators, producing measurement points at the fundamental frequency and harmonics of the resonators. Results of a similar uniformity were obtained for other materials characterised during the programme.

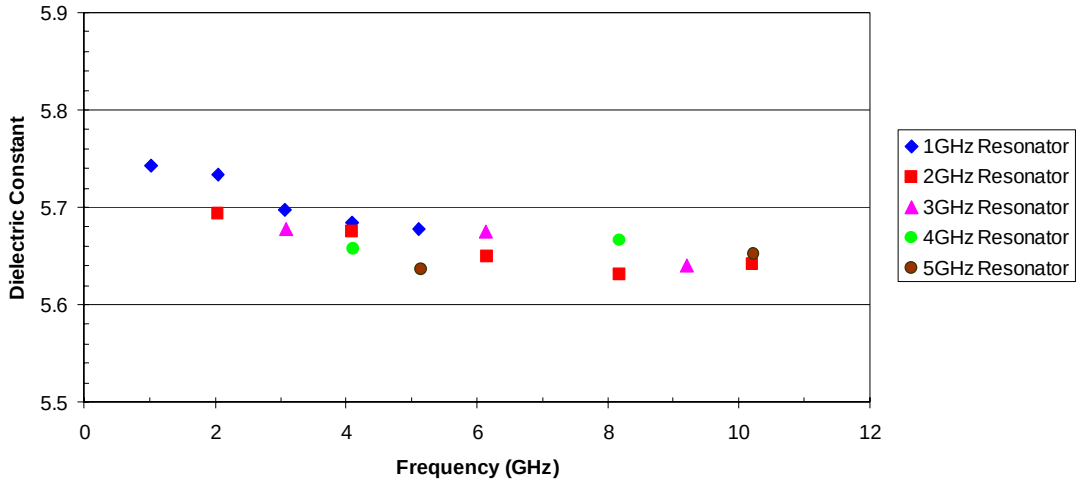

Figure 1: Measured ε_r of Ferro A6 from Ag metallisation resonators

Overview of DRO Design Approach

A DRO uses a dielectric resonator (also known as a "puck") to set the oscillating frequency. The dielectric resonator is a small disc of high permitivity, low loss material that has a fundamental resonant frequency set by its relative dielectric constant (ε_r) and its physical dimensions. Its resonance is a result of reflections at the air/dielectric boundary, in an analogous manner to the resonance of metallic cavities. The resonant frequency is also affected by the presence of grounded metal walls in close proximity. A more detailed explanation of dielectric resonators and their applications can be found in [2].

In order to utilise a dielectric resonator to set the frequency of a microwave oscillator it is normally placed in close proximity to an unshielded transmission line. The transmission line is coupled to the puck, which can be conveniently modelled as a parallel RLC resonator. The typical configuration of the puck coupling to a microstrip transmission line is depicted in Figure 2 together with the electrical equivalent circuit. A transformer is used to model the coupling between the dielectric resonator and the transmission line. The closer the dielectric resonator is to the microstrip line, the higher the turns ratio of the transformer.

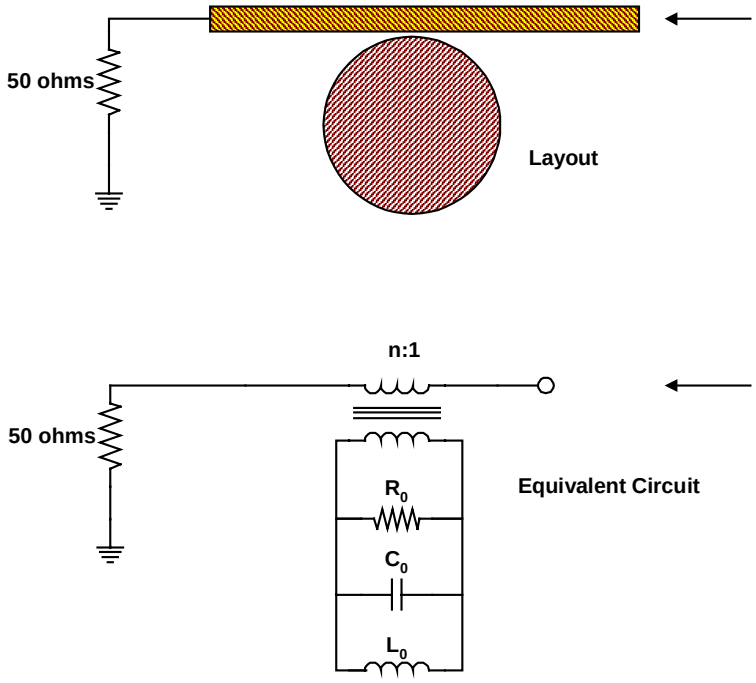

Figure 2: Typical configuration of the dielectric resonator in a DRO

Because the puck is a high Q (low loss) resonator the value of R_0 is very high (typically tens of kΩ) and the phase noise of the resultant oscillator is low. At resonance the reactance of the L and the C are equal and opposite and the equivalent circuit of the dielectric resonator is simply the high value resistor R_0. The frequency of resonance is thus given by Equation 1.

Equation 1: $$F_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L_0 \cdot C_0}}$$

The oscillator is formed by joining the resonator to a negative resistance block. The negative resistance block was realised by applying capacitive feedback to the source terminal of a low noise GaAs FET. The FET is unstable and amplified thermal noise is subject to positive feedback causing oscillation to build up from the noise until a steady state oscillation is reached. Using a bipolar transistor in the negative gain block would have yielded a lower phase noise oscillator but discrete BJTs capable of oscillating at 20GHz were not readily available.

The simplified equivalent circuit of the negative resistance block is shown in Figure 3. A self-bias resistor was used to set the Ids of the transistor and so allow operation without a negative bias voltage for the gate of the FET. The feedback capacitance (C_{fb}) is realised as a printed pad. The inductor (L_{choke}) is realised as a printed high impedance transmission line and is used to ensure that the self bias resistor (R_{sb}) is connected to the transistor through a high impedance at microwave frequencies.

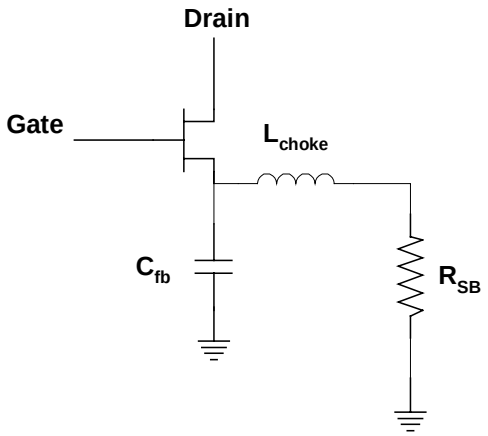

Figure 3: Simplified equivalent circuit of the transistor with feedback

The frequency of the oscillator is primarily set by the resonator. At frequencies below the resonant frequency given by Equation 1, the equivalent circuit of the resonator is predominantly inductive and provides a low reactance path to the 50Ω damping resistor. This resistor prohibits oscillation. At frequencies above the resonant frequency, the equivalent circuit is predominantly capacitive and it is now capacitive coupling that provides a low reactance path to the 50Ω damping resistor. Thus the oscillation is forced to occur at the resonant frequency, as defined in Equation 1, when there is a high impedance path to the damping resistor.

The DRO module has a differential output and this was realised by using two oscillating transistors, each coupled into either side of a single puck. Printed transmission lines connecting each of the negative resistance blocks to the 50Ω damping resistors pass either side of the centrally located puck. The fact that the lines are coupled into the opposite sides of the puck ensures that the outputs of the two oscillating transistors are in anti-phase. This topology is depicted in the final schematic of the complete DRO, shown in Figure 4.

All biasing and decoupling components are included in the schematic. The annotated resistors and capacitors are 0402 SMT components. The resistors without annotation are thick film printed resistors formed as part of the LTCC fabrication process. U1 is a bare Si die voltage regulator IC. Each of the RF outputs of the module is routed through a printed coupler. Its purposes are two fold:

- To reduce the output power to the required level
- To provide buffering and so reduce the effects of load-pulling

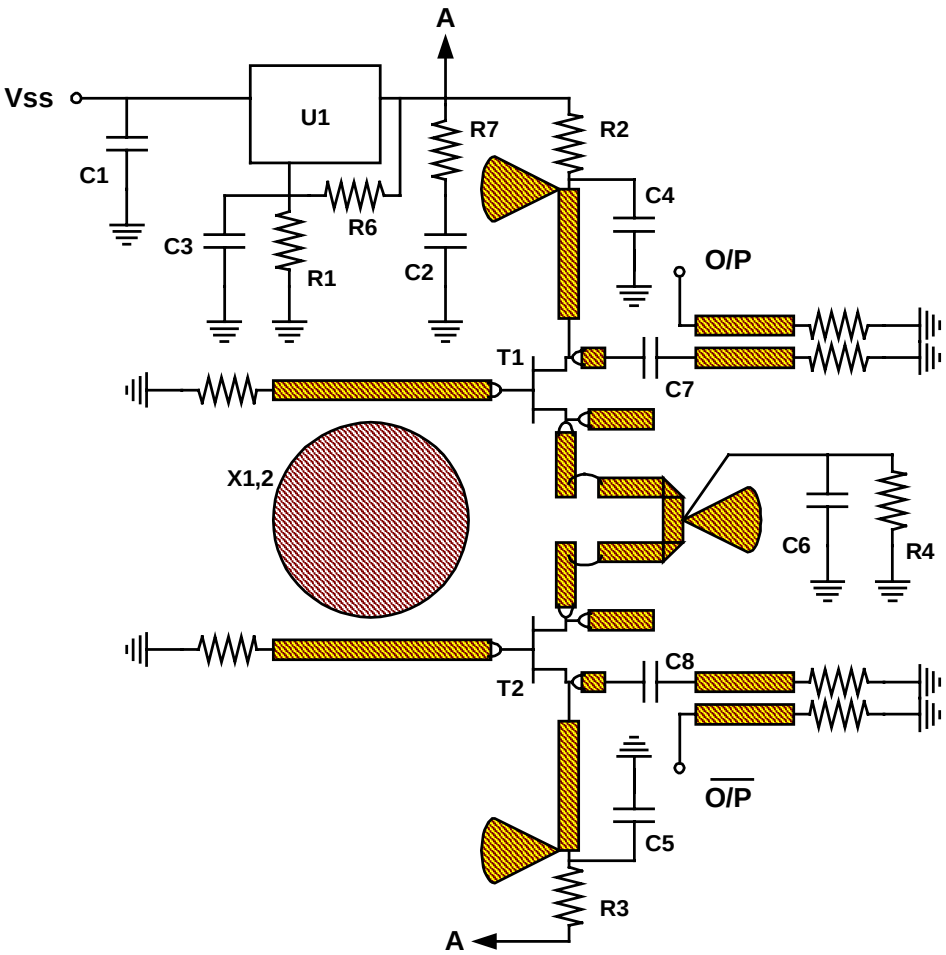

Figure 4: Final schematic of the complete DRO

Detailed Design and Simulated Performance

The oscillator simulations were based around small signal s-parameter data for the transistor. A large signal model of the transistor was not available and so it was not possible to carry out large signal oscillator simulations. Small signal simulation of an oscillator is based around ensuring that the following two conditions hold true at the desired frequency of oscillation:

- There is excess negative resistance
- The total reactance goes to zero

The excess negative resistance is required to allow oscillations to build up. When the oscillations reach steady state the excess negative resistance will actually be zero. With the DRO configuration described above, the damping resistor ensures that there is no excess negative resistance at other frequencies where oscillation could occur, outside the resonant frequency of the puck. Setting the reactance to zero is simply a matter of ensuring that the puck is placed at the correct position in relation to the oscillating transistors.

The analysis approach adopted is depicted in Figure 5. In this case the primary windings of an ideal 1:1 transformer are placed in series between the resonator and the negative resistance block. The transformer does not form part of the oscillator circuit but is included only to allow the analysis of the closed loop oscillator impedance. The real part of the impedance looking into the transformer shows the excess negative resistance. The imaginary part of the impedance is obviously the reactance.

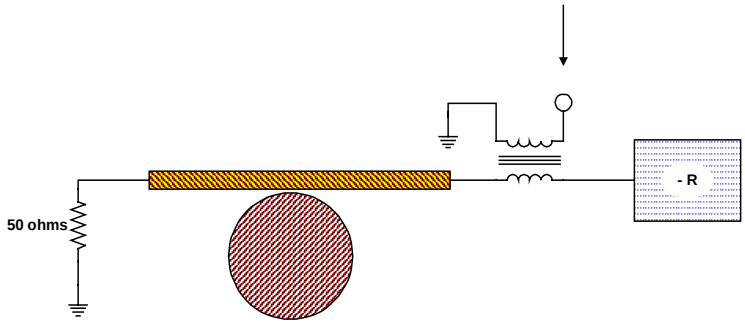

Figure 5: Use of an ideal transformer to analyse negative resistance

An initial simulation was carried out to determine the optimum value of the capacitive source feedback required to configure the FET to exhibit negative resistance. This was determined by observing the magnitude of the reflection coefficient at the gate terminal of the transistor with the drain terminal connected to a 50Ω load. Negative resistance is indicated by the magnitude of s11 being greater than unity. In a small signal oscillator design, it should be a minimum of 1.2, ideally symmetrically centred on the frequency of oscillation. Figure 6 shows the results of this simulation clearly demonstrating adequate negative resistance at the frequency of interest.

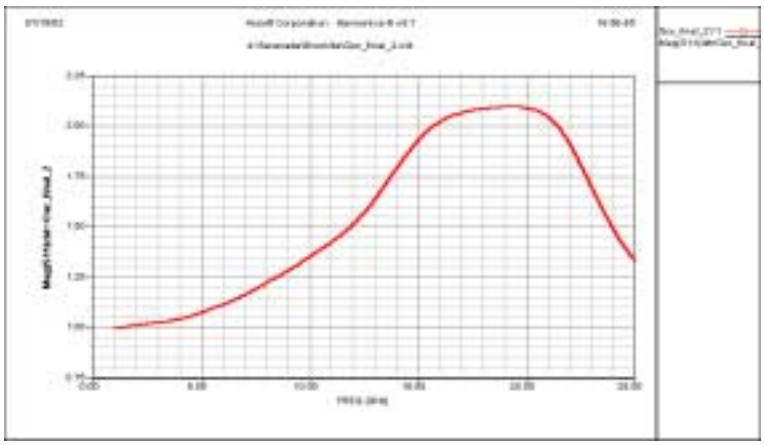

Figure 6: Simulated Mag s11 of transistor with feedback

With the capacitive feedback set, the negative resistance block can now be mated with the resonator to form the oscillator configuration shown in Figure 5. During the initial simulations a simplified resonator was used to ensure that the level of excess negative resistance is present at the required

frequency. The simple resonator was an open circuit microstrip line nominally a quarter wavelength long.

Once adequate excess negative resistance is confirmed with the simple resonator, appropriate models for biasing and decoupling components was included. Care must be taken to model these components and their parasitics accurately as they can give rise to spurious responses in the final oscillator characteristics. However, with careful design these networks should not significantly affect the performance of the oscillator circuit.

The next step was to add the output network. This consisted of a DC blocking capacitor and coupler with thick film resistor terminations. An estimate of the output power was made in order to determine the required coupling ratio of the output coupler to achieve the required output power of around 0dBm nominal for each differential output (+3dBm output power in total). A simulation of the coupler response is shown in Figure 7. This includes thick film resistor terminations on the through and isolated ports. A coupling value of approximately 12.5dB is achieved at 20GHz.

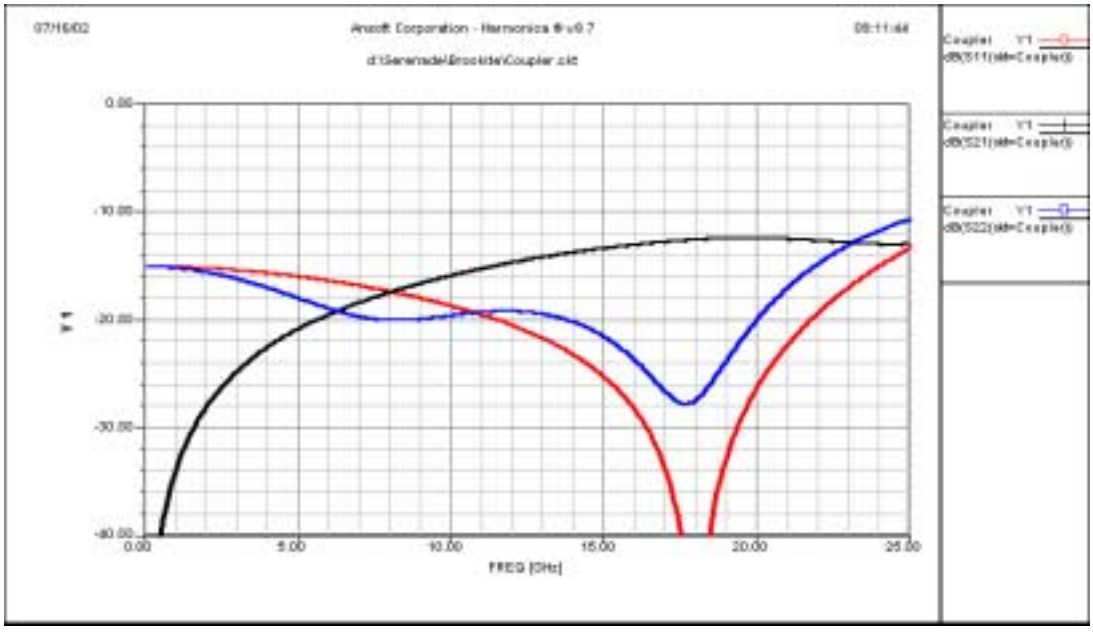

Figure 7: Simulated response of coupler

A photograph of the output network is presented in Figure 8 showing the blocking capacitor, coupler and terminating film resistors.

The next step in the design process was to incorporate the model for the dielectric resonator into the simulation. This would show the effects of the practical model for the thick film damping resistor and allow the length of the gate line required between the transistor and the resonator to be determined.

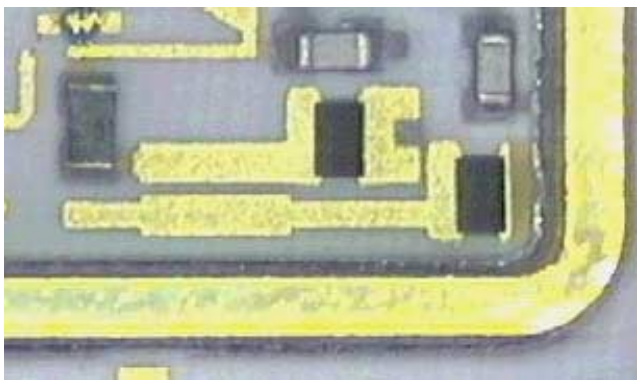

Figure 8: Photograph of the output network

The material chosen for the dielectric resonator had a relative dielectric constant of 30 and a Q of >10000 at 10GHz. Tuning of the oscillator to the required frequency was achieved by selecting the physical dimensions of the puck and the proximity of the metal lid of the cavity. The

closer the metal lid is to the puck the higher the frequency. However, as the lid gets closer to the puck the rate of change of frequency increases and the phase noise degrades.

The turns ratio of the transformer that models the coupling of the dielectric resonator to the microstrip line (Figure 2) is dependent on the proximity of the resonator to the microstrip line. The closer the resonator is to the microstrip line, the higher the coupling and so the higher the turns ratio of the transformer. The level of the coupling, and so the required turns ratio of the transformer, was determined using the computer program CARD from TransTech [3].

The simulated closed loop impedance of the complete DRO is shown in Figure 9. The conditions required for oscillation are seen to be only present at the required frequency of 21.3GHz. A magnified view of the response at the frequency of interest is shown in Figure 10. The excess negative resistance at 21.3GHz is around -7Ω and the reactance is zero, thus meeting the conditions for oscillation.

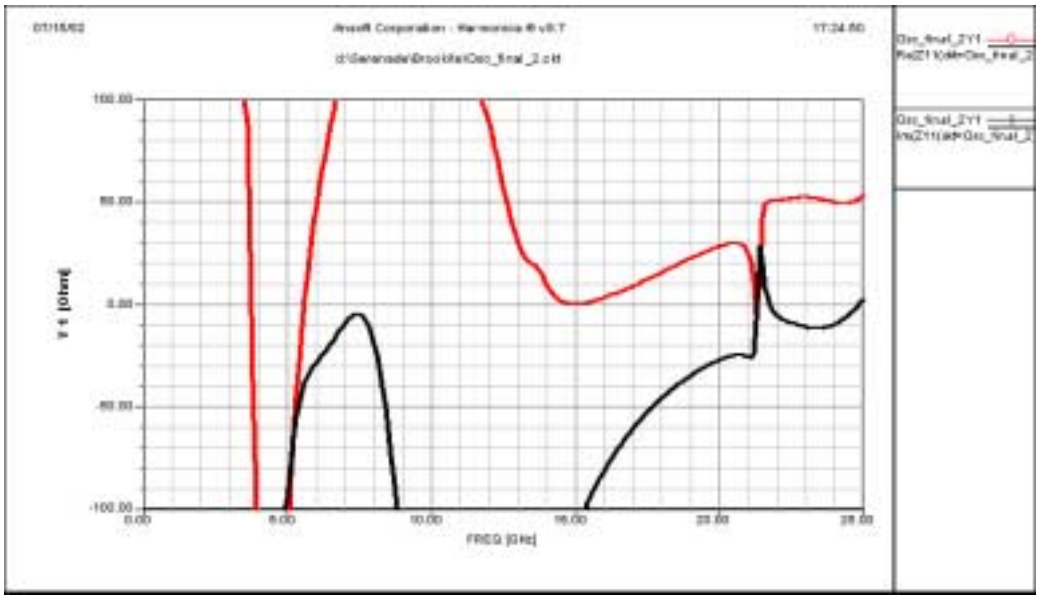

Figure 9: Simulated broadband response of 21.3GHz oscillator

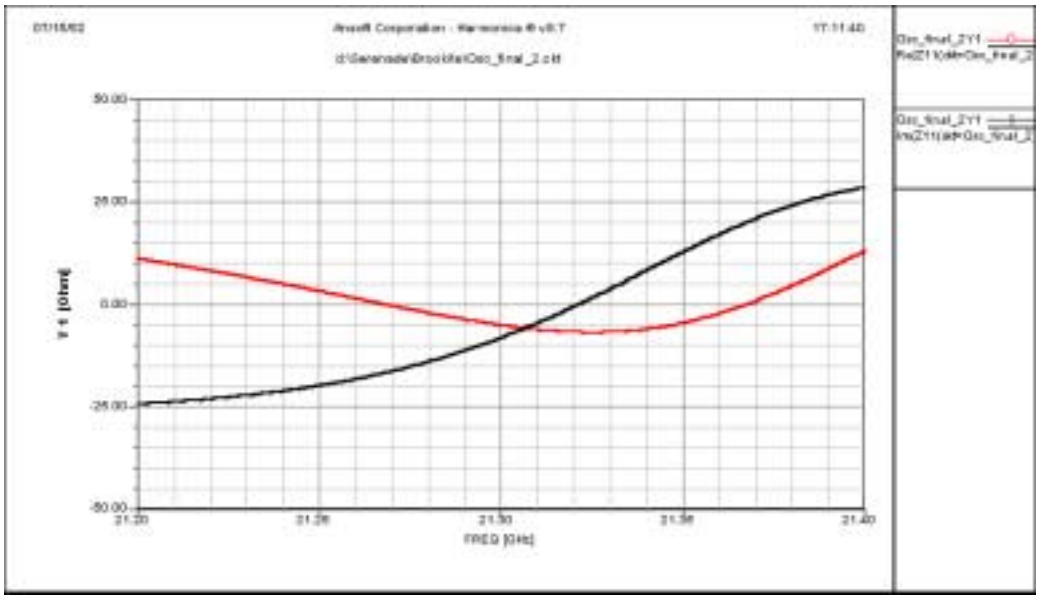

Figure 10: Simulated narrowband response of 21.3GHz oscillator

Simulation of the phase noise of the oscillator was not possible as this requires a non-linear device model and noise parameters.

Module Fabrication

A photograph of one of the DRO's is shown in Figure 11. The oscillators were realised on Ferro A6 LTCC and fabricated by C-MAC Microtechnology. The components used were a mixture of bare die together with SMT and printed passives. The bare die are mounted onto the LTCC tile with conducting epoxy and gold wire bonded. The SMT components are solder attached. A total of six thick film printed resistors were used. These were all for terminating loads and can be identified as the black rectangles in Figure 11.

The large circular dielectric resonator is positioned centrally. The printed lines running either side of the resonator couple into it and so the frequency of oscillation is set. The black rectangles at the ends of these lines are the printed damping resistors to prevent unwanted oscillations at other frequencies. The voltage regulator, a bare die Si part, can be seen in the top left corner.

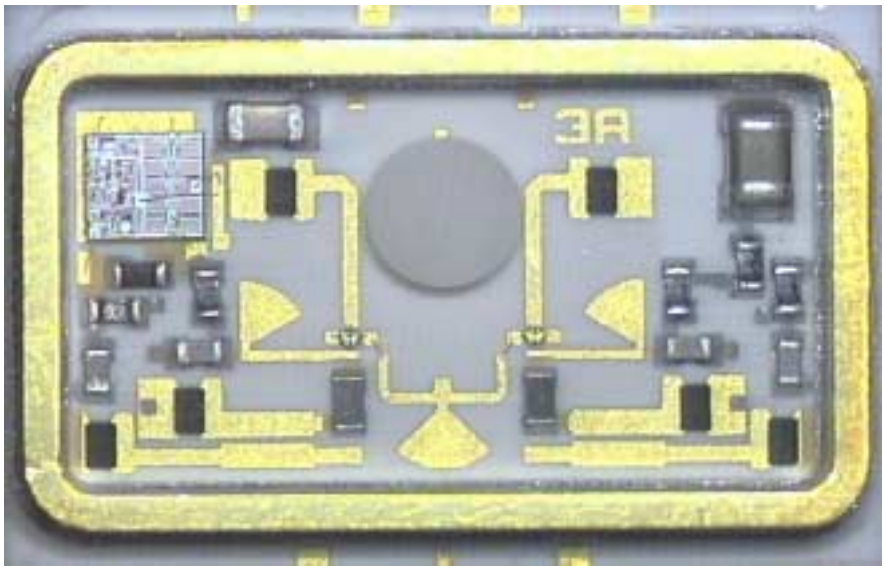

Figure 11: Photograph of one of the DRO's

Measured Performance

The DROs were measured in purpose built test jigs. One of the two differential outputs was terminated in a 50Ω co-axial load whilst the other was measured. The plots shown below were taken directly from the spectrum analyser and no account of cable and jig losses are included. The insertion loss of the cable connecting the test jig to the spectrum analyser was measured as 1.2dB at 20GHz. The loss of the test jig is estimated at a further 0.2dB. Thus a correction factor of 1.4dB must be added to the power measurements on the spectrum

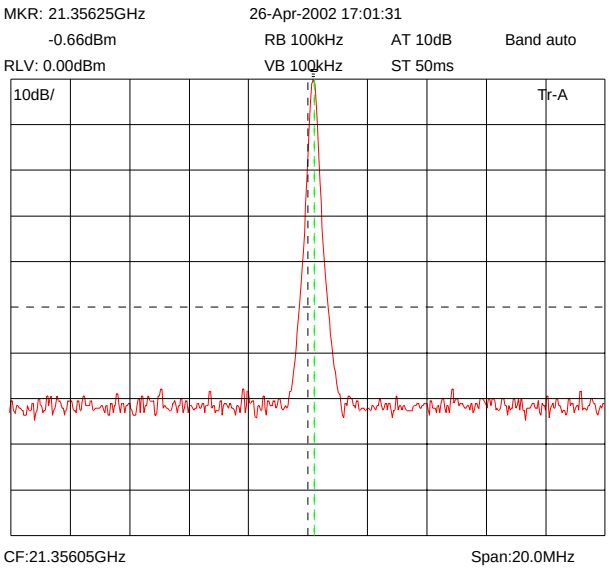

Figure 12: Oscillator port 1 output spectrum

analyser plots.

Figure 12 shows the measured output spectrum of port 1 of one of the DRO's. The oscillation frequency is 21.356GHz and the indicated power level is –0.7dBm so accounting for the loss of the test jig and cable, the actual power from this port of this oscillator module is +0.7dBm. Figure 13 shows the measured output of port 2, which is approximately –0.8dBm. Taking the loss of the test jig and cable into account, the power from this port of this oscillator module is estimated at +0.6dBm.

The phase noise of the oscillators was measured, using a spectrum analyser, to be -102dBc/Hz at 100kHz.

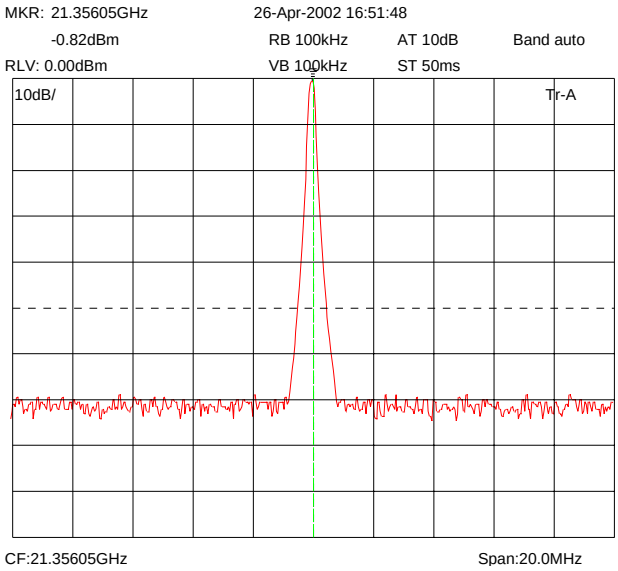

Figure 13: Oscillator port 2 output spectrum

Conclusions

The design fabrication and evaluation of an LTCC based differential DRO module has been described. Ferro A6 material was used and the module includes bare die, SMT components, printed couplers and printed resistors. The DRO operates at 21.3GHz has an output power of just over +3dBm with an amplitude imbalance between the output ports of < 0.2dB and a phase noise of –102dBc/Hz at 100kHz offset from carrier. The module is the prototype of a commercial product that is now under development. The commercial product will also include a small voltage tuning range to allow phase locking of the DRO for applications such as clock generation in 40Gb/s optical transceivers.

References

[1] Liam Devlin, Graham Pearson, Jonathon Pittock, Bob Hunt, "RF and Microwave Component Development in LTCC", proceedings of the 38th Annual IMAPS Nordic Conference, Oslo, Norway, September 2001, pp 96-110

[2] D. Kajfez and P. Guillon, P. "Dielectric Resonators", Second edition, Noble Publishing, 1998 ISBN: 1-884932-05-3

[3] Computer Aided Resonator Design – CARD Version 3.2; ScillaSoft Consulting/TransTech