MMIC Design for Wireless Broadband Access

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Abstract

This paper describes the design and development of GaAs Monolithic Microwave Integrated Circuits (MMICs), for use in a range of wireless broadband access systems. The examples covered are a Power Amplifier (PA) for 5.2/5.8GHz U-NII applications (including IEEE 802.11a), a low cost broadband (Darlington pair) amplifier for use in Ultra-WideBand (UWB) systems, and several different MMICs for use in mm-wave Broadband Wireless Access (BWA) systems.

Introduction

GaAs-based MMICs are widely used in telecommunication products from frequencies below 1GHz to mm-wave applications at 60GHz and beyond. A wide range of device technologies is available, each with particular advantages. These include:

- InGaP Heterojunction Bipolar Junction Transistor (HBT) processes, which find wide commercial adoption for high power and high linearity RF amplifiers, and low-cost broadband amplifiers.
- Pseudomorphic High Electron Mobility Transistor (pHEMT) processes, which are favoured for active mm-wave circuits and high power RF switches.
- Vertical PIN diode processes, which have very low parasitic capacitance and find applications in mm-wave switches and broadband limiters.

This paper describes examples of MMICs designed using all of the above technologies, covering operating frequencies from DC to 45GHz.

4.9-6GHz PA for U-NII applications including 802.11a

This circuit is a two-stage class AB design that uses a novel current-mirror based active bias circuit, to optimise bias current with drive level, and to extend the linear gain region of the amplifier [1]. A photograph of the MMIC is shown in Figure 1 and a simplified circuit schematic is shown in Figure 2.

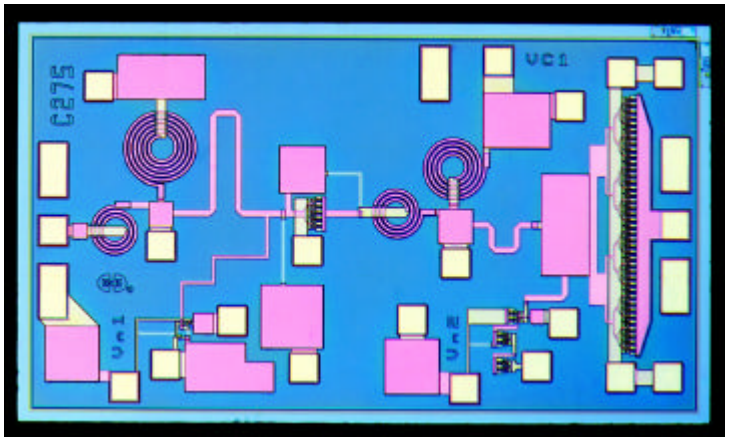

Figure 1: Photograph of the U-NII PA

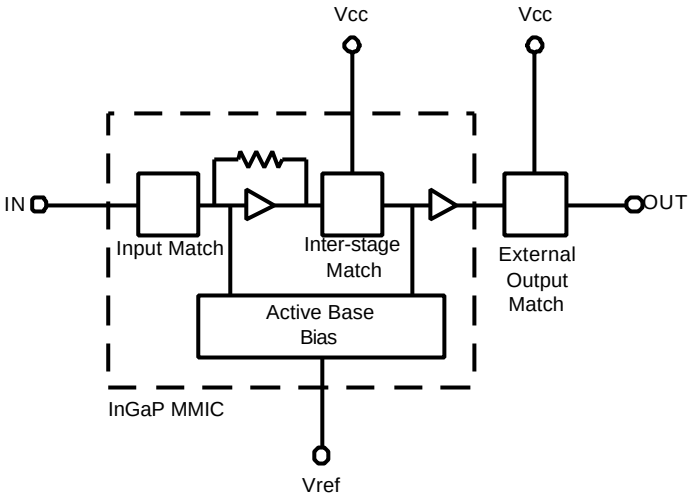

Figure 2: Simplified schematic of the U-NII PA

The first stage of the amplifier uses series resistive feedback for improved stability and has an on-chip integrated input matching network. The second stage is a large HBT device (40 x 42μm^2 emitter fingers), with a collector-coupled output. Inter-stage matching is included on-chip between the two stages. Different configurations of active bias circuit are used to control the base currents of the two stages, with each incorporating a linearising capacitor to improve linearity when the amplifier is operated backed-off from compression. The effect of optimising the values of the two linearising capacitors is best illustrated by Figure 3.

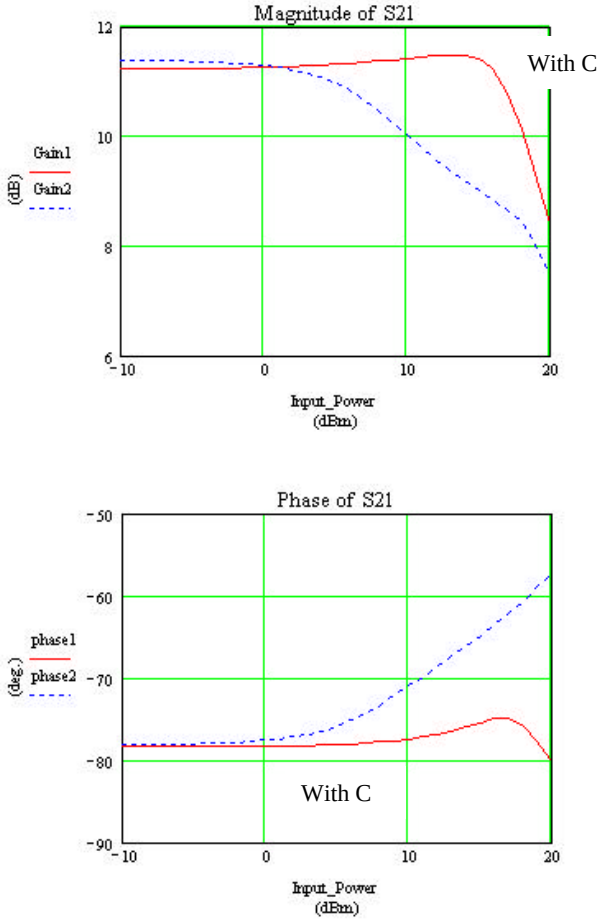

Figure 3: Effect of linearising capacitors on the magnitude and phase of the gain

The graphs of Figure 3 show the simulated magnitude (in dB) and phase (in degrees) of the transfer characteristics (gain) of the output stage, biased through its active bias circuit, with and without the linearising capacitors. Without the capacitors (blue dotted traces) both the magnitude and phase of the gain become highly non-linear with respect to the input power drive level, well before saturation occurs. With the optimum value capacitors in place (red solid traces), the gain and phase remain linear right up until the device begins to saturate.

An external bias tee is required to bias the collector-coupled output and this is incorporated into a simple discrete LC output matching network. The measured small-signal gain of the amplifier is just below 18dB at 5.25GHz, falling to 17dB at 5.85GHz. The output return loss is better than 13dB across the 4.9 to 6GHz band (with simple off-chip matching), and the on-chip matched input has a return loss of greater than 10dB. The measured power transfer characteristics (at 5.25 GHz) are illustrated in Figure 4. It can be clearly seen that when the amplifier is operated at an output power level of +18dBm it is backed off by approximately 8dB from 1dB compression, the gain is very flat and the current drain is much less than that at power compression.

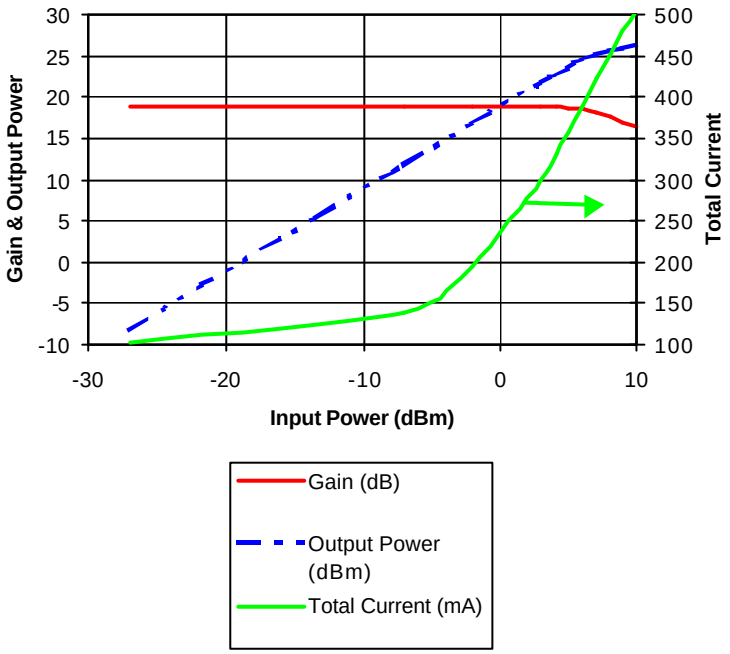

Figure 4: Measured performance of the U-NII PA versus input power

Low-cost broadband amplifiers for UWB

Small-size (and so low-cost) broadband DC coupled amplifiers can be designed using a Darlington transistor pair configuration [2]. A simplified schematic of the design described here is shown in Figure 5. The RF output is collector-coupled and a DC supply voltage is applied through an external bias tee that includes a resistor for stabilisation of the bias current.

The on-chip resistors are selected to both bias the transistors to the required operating point and to optimise the RF performance. The RF performance is optimised to achieve a flat gain response with input and output impedances of 50Ω. Series resistive feedback is used on the output stage (Re2), together with a small amount of series inductive feedback (Le2), to improve the high frequency match whilst simultaneously setting the required bias. Shunt resistive feedback around the whole amplifier (Rfb) is also combined with inductance (Lfb). This serves to reduce the effect of the shunt resistive feedback at the top of the band, so increasing the amplifier gain and flattening the overall gain versus frequency response.

The operational bandwidth of the IC can be extended significantly by the use of simple external matching using conventional, low-cost 0402 components [3]. The matching is realised by optimising the values of the DC blocking capacitors and the bias inductor L1. An additional capacitor is also required to provide an RF ground for L1 so that it acts as a shunt matching component. The component values are chosen to reactively match the amplifier at the top end of the band, so increasing the return loss and gain. The DC blocking capacitors are reduced significantly in value, which increases the amplifier's low frequency cut-off. However, the upper operating frequency can be extended by 4GHz.

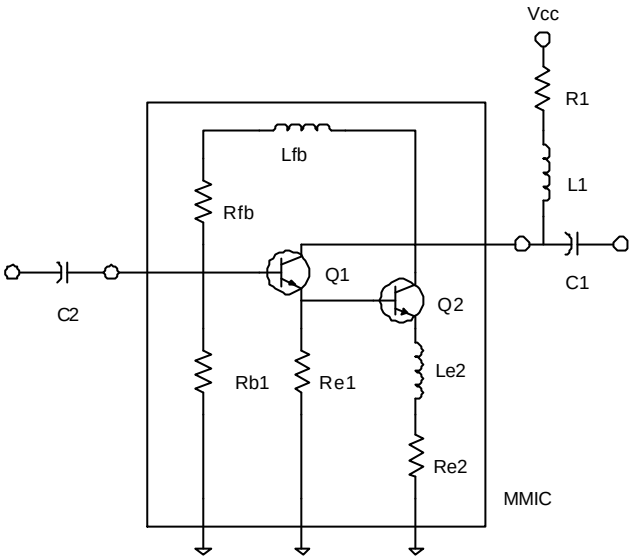

Figure 5: Simplified schematic for the broadband Darlington pair amplifier

The measured performance of the broadband amplifier is shown without external matching in Figure 6 and with external matching in Figure 7. Without matching the low frequency gain is 11dB, rolling off gently with frequency to give a 3dB bandwidth of 9GHz. Input and output return losses are both greater than 10dB to 9GHz. The addition of the external matching allows the operational bandwidth of the amplifier to be extended to 13GHz. In this case (Figure 7) the gain is just under 9dB at 4GHz falling to just below 7dB by 12GHz with an output return loss of greater than 13dB. It should be noted that no specialist microwave components were required to achieve this performance.

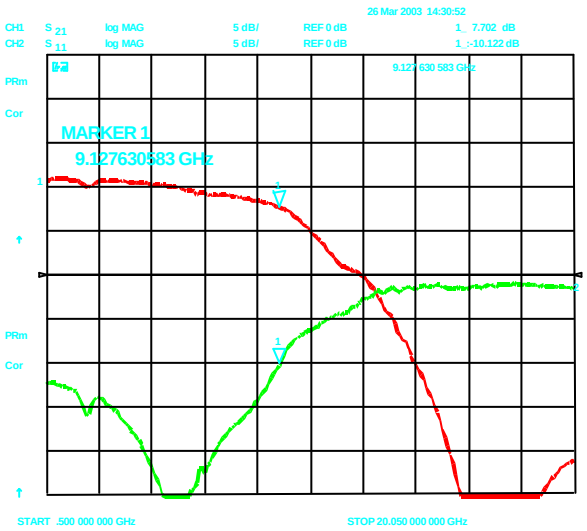

Figure 6: Measured small-signal response of broadband amplifier without external matching

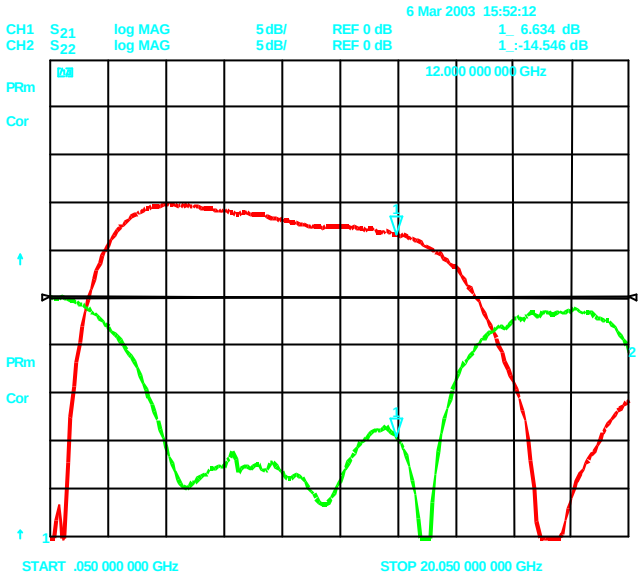

Figure 7: Measured small-signal response of broadband amplifier with external matching

A comparison of the measured versus simulated power transfer characteristics at 4GHz is shown in Figure 8. The 1dB gain compressed output power level is 11.5dBm and excellent agreement between measured and modelled performance is demonstrated.

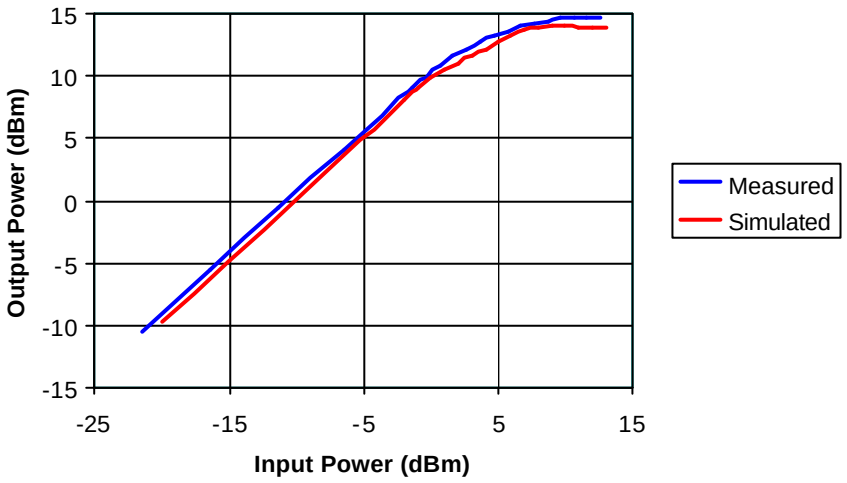

Figure 8: Power performance of broadband amplifier

MM-wave MMICs for Broadband Wireless Access

Short gate length pHEMT transistors have high values of Fmax and are therefore commonly used for the realisation of active mm-wave circuits. Diode based processes are often used for the realisation of passive mm-wave mixers (normally using Schottky diodes) and switches (normally using PIN diode based processes). Examples of mm-wave MMICs for BWA systems, designed using both pHEMT and VPIN processes, are shown below.

43GHz Gilbert Cell Mixer

Gilbert-cell mixers [4] are active switching mixers that are used almost universally for the realisation of mixing functions on RF bipolar ICs. The design described here uses the same approach on a commercially available 0.25μm gate length pHEMT process to realise a compact, low-loss downconvert mixer at 43GHz. For minimisation of chip area a half Gilbert-cell configuration was chosen. An on-chip passive, lumped element balun was used for differential combination of the IF output, which was at around 5GHz. A simplified schematic of the mixer is shown in Figure 9.

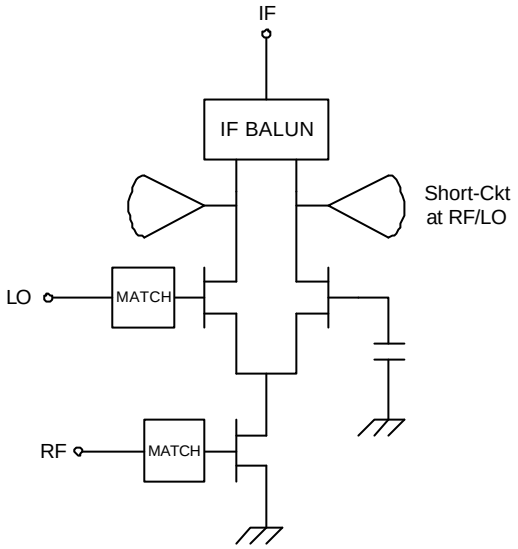

Figure 9: Simplified schematic of the mm-wave Gilbert-cell mixer

The RF input is matched to the bottom transistor to provide low noise figure. The LO signal is matched to the input of one of the differential pair of transistors that sit above the RF input transistor. The input of the other transistor in the pair is grounded through an on-chip via, which avoids the use of an LO balun, thus saving chip area and therefore cost. The bottom (RF) transistor of the tree also acts as a current source to bias the differential pair. The top of this current source is high impedance to the LO signal, which is shared across the differential pair, so switching them in anti-phase.

A photograph of one of the mixer ICs is shown in Figure 10. The layout of the IC was purposely extended in order to allow fabrication as part of a multi-chip array also containing other designs. In production the chip area would be substantially reduced. The mixer's conversion loss is a strong function of LO drive level as can be seen in the measured performance plot of Figure 11. At 43GHz the conversion loss is 4.2dB with +10dBm drive, 7.6dB with +5dBm drive, and 13dB with 0dBm drive. The large signal simulations show good agreement with this measured performance [5]. The losses are lower than would be expected with Schottky diode mixers with similar LO drive levels.

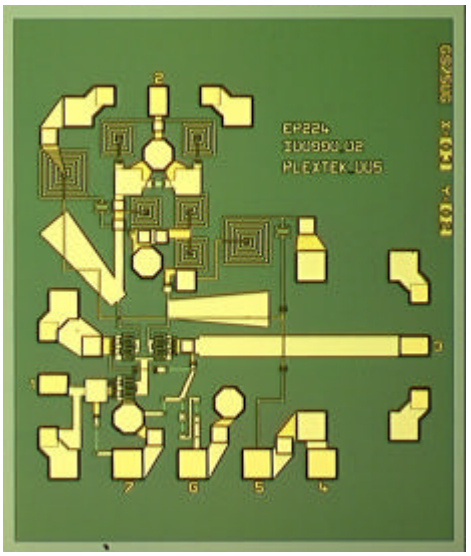

Figure 10: Photograph of the mm-wave Gilbert-cell mixer

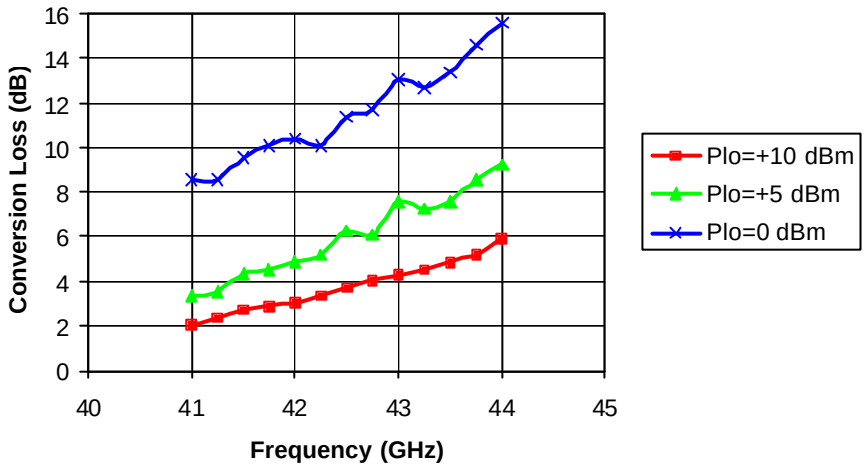

Figure 11: Measured conversion loss at various LO power levels

13GHz (to 39GHz) pHEMT Trebler

The frequency trebler IC was designed as an LO frequency multiplier. It was fabricated on the same commercially available 0.25µm gate length pHEMT process as the mixer. The topology is essentially a single stage overdriven amplifier, which allows the chip area to be minimised and therefore produces the lowest cost approach. The pHEMT device was biased in class A for optimum performance in trebler mode [6] using a self-bias technique to enable operation from a single positive supply.

An on-chip matching network centred at 13GHz was included at the input of the transistor to maximise power transfer at this frequency. The output matching network was centred at 39GHz. As well as providing a power match for the 3rd harmonic output, it also provided the correct terminating impedance at the fundamental and second harmonic. A further design goal was to provide adequate rejection of the sub-harmonics so that their output levels were acceptable.

A photograph of the fabricated chip is shown in Figure 12. The measured conversion loss versus frequency is shown in Figure 11, the minimum value being 6dB at 39.75GHz. The measured rejection of the fundamental input signal was greater than 22dB at this frequency. The required DC bias current was 30mA from +5 Volts.

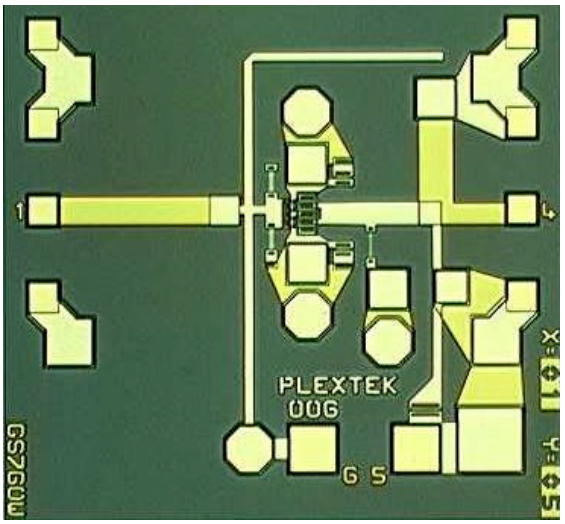

Figure 12: Photograph of the pHEMT MMIC trebler

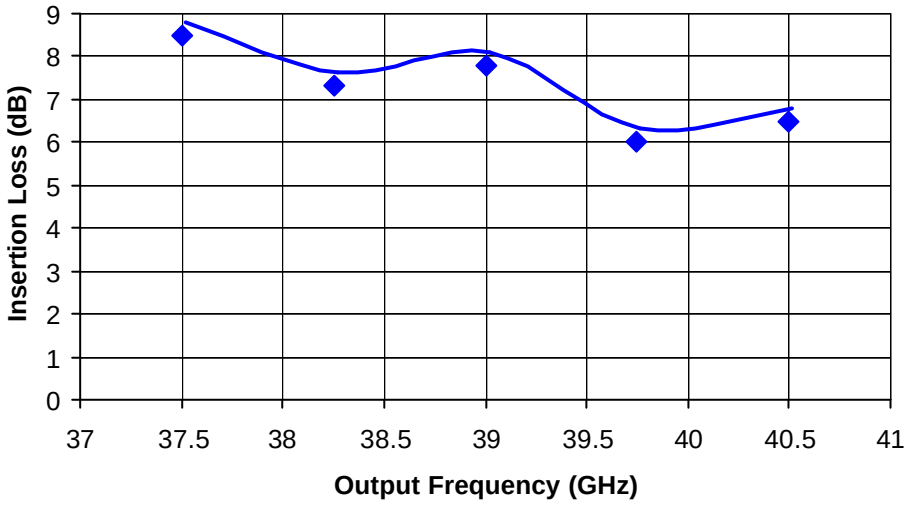

Figure 13: Measured conversion loss of frequency trebler versus output frequency

24-34GHz and 34-45GHz Switches

The VPIN process of TriQuint-Texas Semiconductor was used for the fabrication of mm-wave Single Pole Double Throw (SPDT) and Single Pole Four Throw (SP4T) switches. The design and performance of the SP4Ts [8] is described here.

The design used only shunt diodes because this allows the lowest on-case insertion loss and because the parasitic off-case capacitance of the diodes means that they offer limited mm-wave isolation when used in series. The approach taken was to absorb the capacitance of the shunt mounted off-state PIN diodes into a low-pass filter. The design approach is illustrated in Figure 14 and culminates in a low pass filter comprising shunt mounted off-state diodes and series, high-impedance transmission lines. Choosing the appropriate number of shunt

capacitors (diodes) in the filter is a compromise between having increased isolation and lower die area/current consumption. In the designs reported here, two shunt diodes were selected.

It is important that the filter is well-matched with low insertion loss when the diodes are off (switch on) and that it presents a high input impedance (with high insertion loss) when the diodes are on (switch off). This allows multiple filters (forming the arms of the switch) to be connected to a common input to form a multi-way switch.

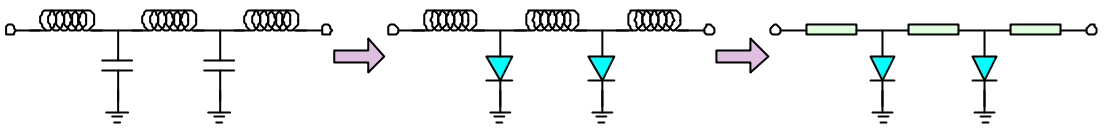

Figure 14: VPIN filter design strategy

Two versions of the SP4T were designed to cover the frequency range 24 to 45 GHz. Each switch has the same circuit topology, shown in Figure 15, but covers different operating bands, namely:

- Low band SP4T: 24 to 34GHz
- High band SP4T: 34 to 45GHz

A photograph of the MMICs is shown in Figure 16. Two 4" diameter wafers of VPIN switch circuits were measured and showed yields of 95%. A summary of the measured performance of the two designs is given in Table 1. Figure 17 compares the measured versus modelled performance of the low-band design and Figure 18 compares the measured versus modelled performance of the high-band design. In both cases very good agreement is demonstrated.

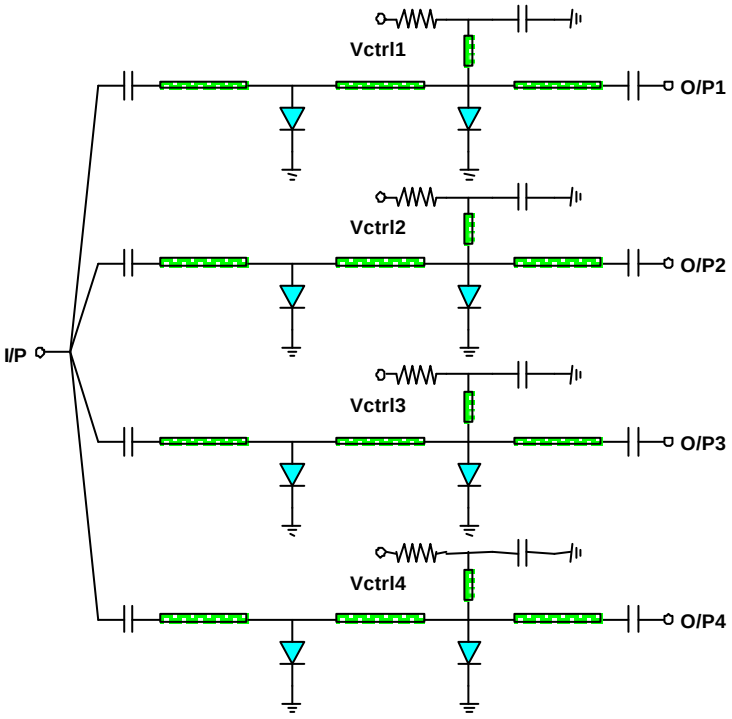

Figure 15: SP4T switch schematic

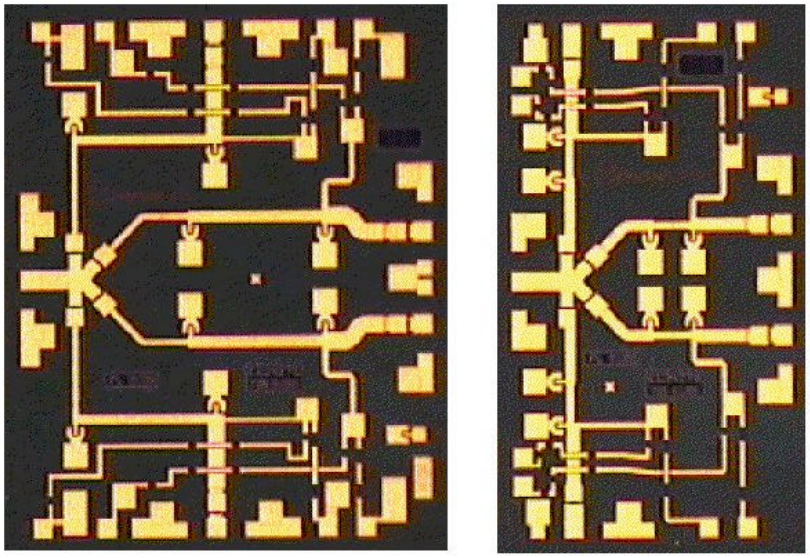

Figure 16: Photograph of the SP4T MMICs (24 to 34GHz design on the left, 34 to 45GHz on the right)

Band ®	24 - 34GHz	34 - 45GHz
On-case loss	1.1 ± 0.3dB	0.75 ± 0.2dB
Off-case isolation	> 19dB	> 24dB
Input return loss	> 15dB	> 14dB
Output return loss	> 19dB	> 17dB

Table 1: Summary of the measured performance of the SP4Ts

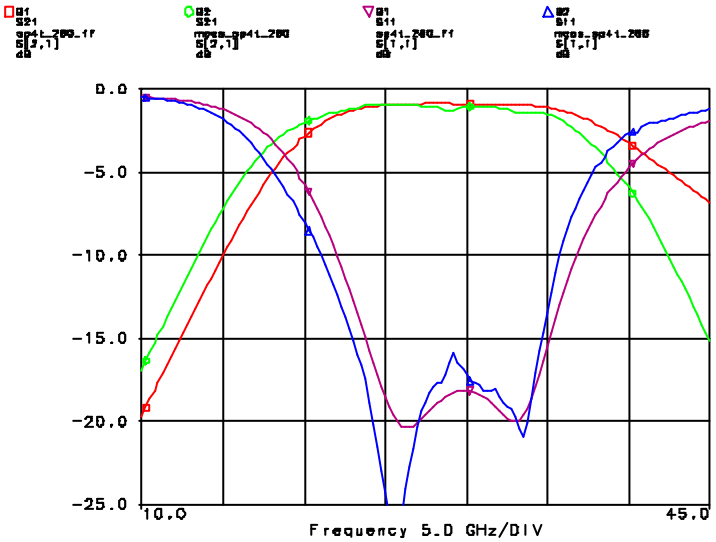

Figure 17: Measured versus simulated small-signal performance of one branch of the low-band SP4T MMIC in the on state

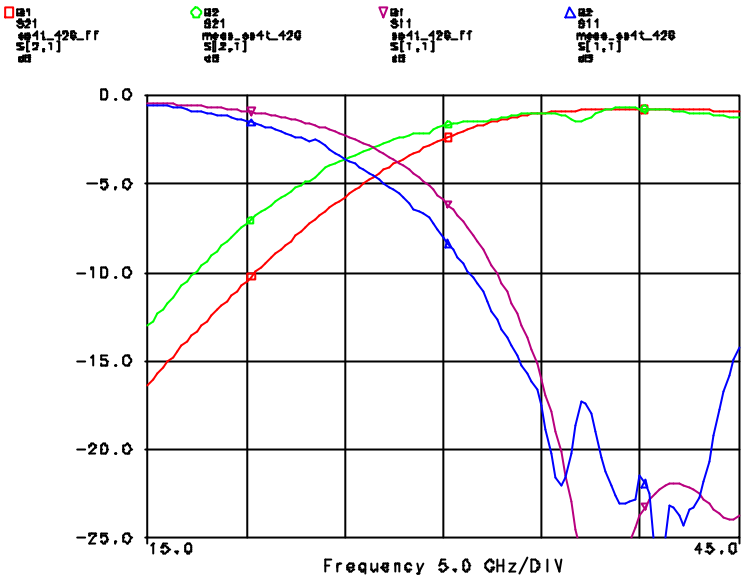

Figure 18: Measured versus simulated small-signal performance of one branch of the high-band SP4T MMIC in the on state

Conclusions

This paper has covered a variety of circuit functions, designed on commercially available GaAs processes, utilising a range of technologies including InGaP HBT, pHEMT and VPIN. The operating frequencies of the ICs range from sub-1GHz to greater than 40GHz and could be used to address many commercial applications including U-NII, UWB and mm-wave wireless access networks.

References

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