OSCILLATORS

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Introduction

The designers of monolithic or integrated oscillators usually have the available process dictated to them by overall system requirements such as frequency of operation or cost. Furthermore the use of high quality resonators such as crystals or ceramic resonators are not entirely compatible with the integration process. Thus the designer loses degrees of freedom in the choice of active device and tank circuits. However, for a given process the advantages for the oscillator designer include the availability of a wide range of active device sizes, and the fact that lumped element components such as R's, L's and C's are not limited to E12/E24 standard values.

This tutorial concentrates on the design techniques for a monolithic GaAs MESFET fixed frequency oscillator at 9.35 GHz, for an X-band Transponder application. The techniques can equally be applied to RF bipolar, CMOS or BiCMOS processes in the MHz region. For certain system applications the relatively poor quality of the monolithic resonator implies that off-chip components must be used. In these cases it is still often worth including a 2-port negative resistance circuit on-chip, so that the end-user merely has to supply a resonator at the desired frequency of operation.

Preliminary Design Concepts

The design process should begin with the choice of active device and suitable bias condition. In this example a 0.5µm gate length/300µm gate width GaAs MESFET is used. The device, part of the MMT F20 FET library, has a gain of the order of 12 dB at 10 GHz. A bias point of Vds=+3V and Ids=50% of Idss is chosen as a fairly standard small-signal bias point. The next step is to apply feedback to the active device in order to cause instability, and thus produce a device exhibiting negative resistance (Ref. 1). The concept of this is illustrated in Figure 1(a). In this example, the aforementioned transistor with a suitable capacitor value in the source yields an input impedance that has a negative real part, and a capacitive reactance. Thus coupling the circuit to a suitable value inductor will yield the simple equivalent circuit of figure 1(b). This circuit will oscillate at the frequency given by;

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad \text{… Eqn. (1)}$$

... if;

i. At the start-up of oscillation there is an excess negative resistance (-R)

ii. At the steady state the positive resistances & -R exactly cancel each other.

For this transistor a monolithic Polyimide capacitor of 0.33pF prime capacitance peaks the negative resistance at 9.35 GHz, the desired frequency of oscillation.

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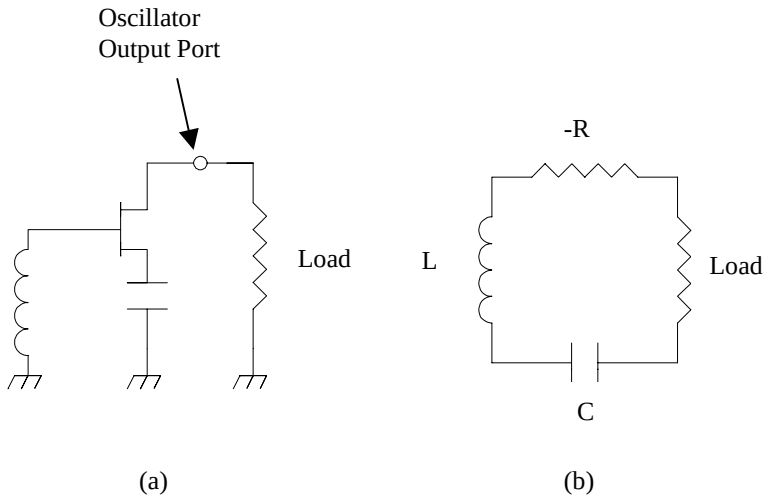

Figure 1: Simple Oscillator Schematic & Equivalent Circuit

Small-signal Design Techniques

A conventional linear RF/Microwave simulator can be used to predict the approximate frequency of oscillation of a negative resistance oscillator. In this tutorial the Serenade® design suite from Ansoft is considered (Ref. 2). The simple fixed frequency oscillator of figure 1(a) is entered into the Serenade Schematic Capture package, as illustrated in Figure 2. The 1-port circuit has the fundamental elements of source capacitor (Cs) and gate inductor (Lg) entered as variables. As previously mentioned the source capacitor is a parallel plate capacitor with Polyimide dielectric. The gate inductor is a planar spiral formed on the top layer of interconnect metallisation. The additional inductors, capacitor and resistor are used for RF choking, DC blocking and self-bias respectively. The load into which the circuit must oscillate (50 Ω) is represented by the 50 Ω port termination. Although the schematic appears relatively simple, each of the MMIC passive models is a complex model in it's own right, incorporating several stray and parasitic elements.

The prime capacitance of Cs has already been established as 0.33 pF, in order to peak the negative resistance at the desired frequency of oscillation (9.35 GHz). The primary gate inductance, Lg, is then swept until the desired frequency of oscillation is obtained. In this case, a value of 2.5 turns for a 12µm planar spiral is determined. The result of the small-signal simulation is presented in Figure 3. It can be seen that the imaginary part of the closed-loop impedance goes through zero at two frequencies namely 9.4 GHz and 11 GHz. At these two frequencies the equation $X_L=X_C$ is solved, yielding the resonant frequency of Eqn. (1). Recall that for oscillation the real part of the impedance needs to be negative. In fact, for oscillation to commence a negative resistance of < -50 Ω is required, primarily to overcome the +50 Ω of the oscillator load. At the 11 GHz point the overall resistance is actually positive. Thus any possibility of oscillating at this frequency is damped out. At 9.4 GHz however, the real part is -137 Ω. This provides ample -R to overcome the load plus any unforeseen parasitic resistances, and provides excess -R for oscillation to build into a steady state.

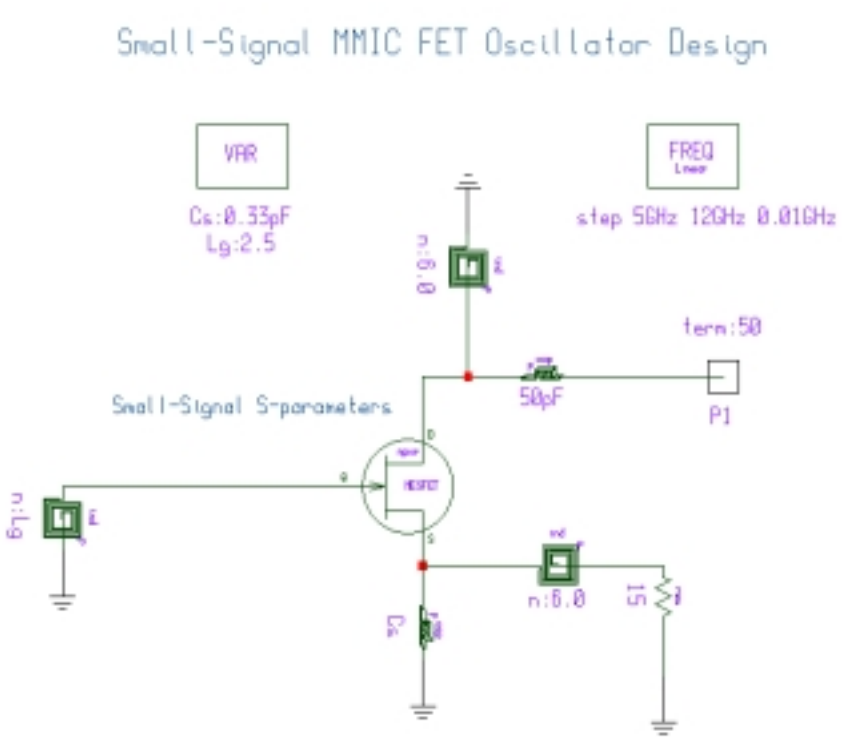

Figure 2: Oscillator Schematic for Small-signal Simulation

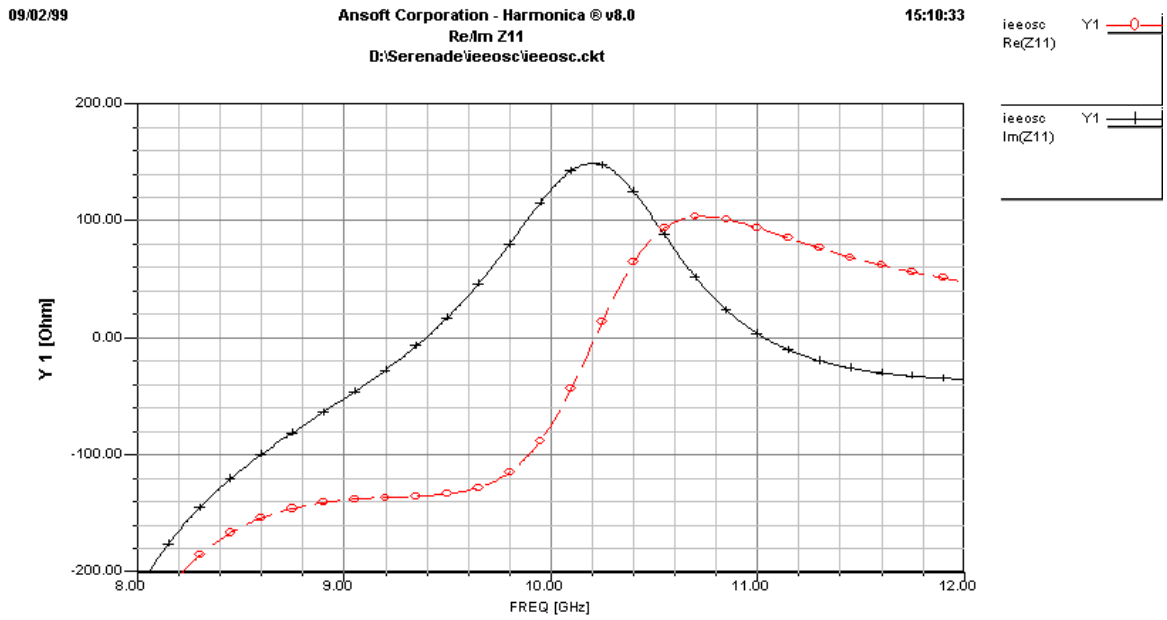

Figure 3: Oscillator Small-signal Simulation

Large-signal Design Techniques

If a more expensive non-linear Harmonic Balance simulator is available, then the true steady state condition for oscillation can be simulated. To do this the previous small-signal schematic is copied into a new schematic. The small-signal model (or measured S-parameters for the device) is replaced by a representative non-linear model. A bias voltage is then applied to the drain of the FET, as shown in Figure 4. A frequency control block showing the range over which the simulator should determine the frequency of oscillation is required, as is the number of harmonics which to analyse. In this case the relatively wide range of 2 to 20 GHz is chosen, along with 3 harmonics. The non-linear output block (NOUT) and the noise model date (.NOI) are required for phase noise analysis.

A quick DC analysis of the circuit shows that a Drain voltage of 3.9V is adequate for a Vds of 3V, and an Ids of 50% Idss, which is the identical bias point as used in the small-signal analysis. The resulting non-linear simulation is best represented by the oscillator output spectrum, as given in Figure 5. This shows a fundamental oscillation frequency of 9.35 GHz, with +11.3 dBm delivered into the 50 Ω load. The relative content of the second and third harmonics are also available. Figure 6 illustrates the output waveform of the oscillation. The contributions of the harmonics in distorting the desired sine wave is clearly visible. Assuming a decent noise model is readily available then the same simulator can be used to predict oscillator phase noise at given offset frequencies. Figure 7 is the result for this particular circuit swept over offset frequencies from 10 KHz to 1 MHz. The value of approximately -75 dBc/Hz at 100 KHz offset is typical for a monolithic X-band oscillator.

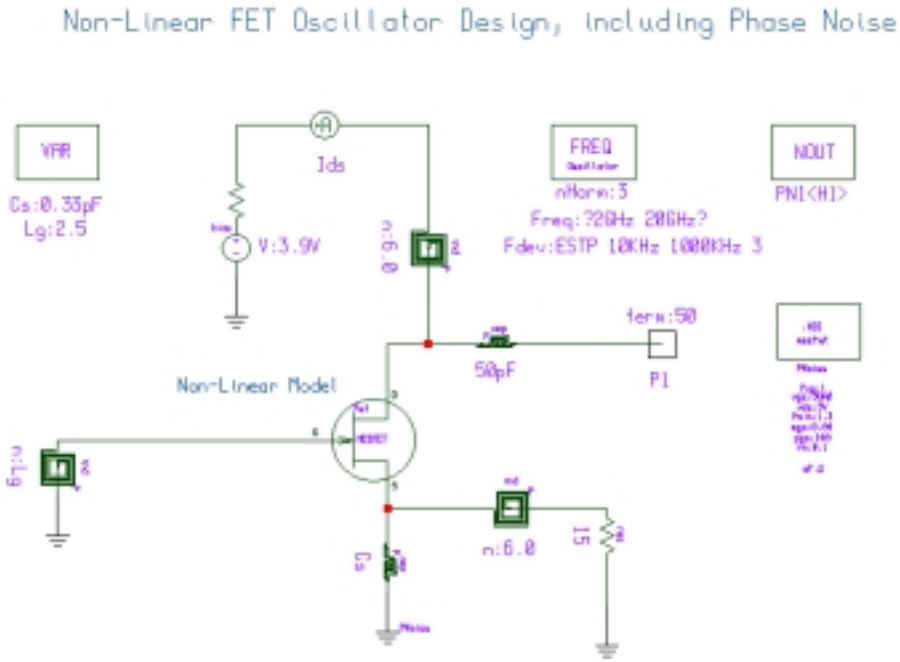

Figure 4: Oscillator Schematic for Large-signal Simulation

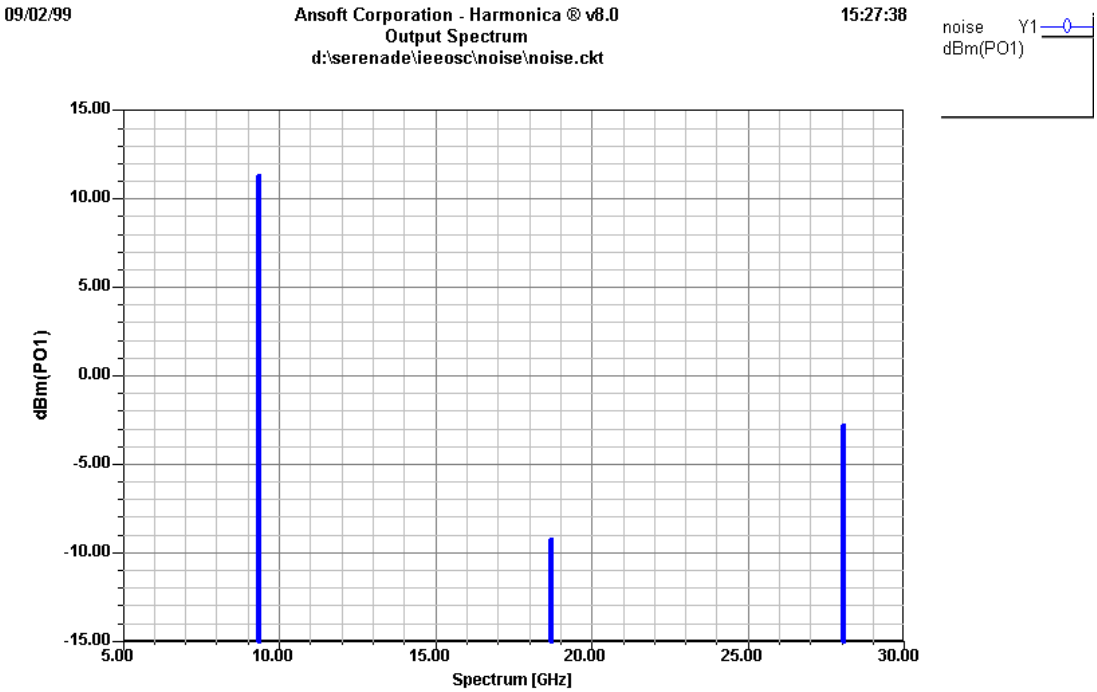

Figure 5: Oscillator Large-signal Simulation

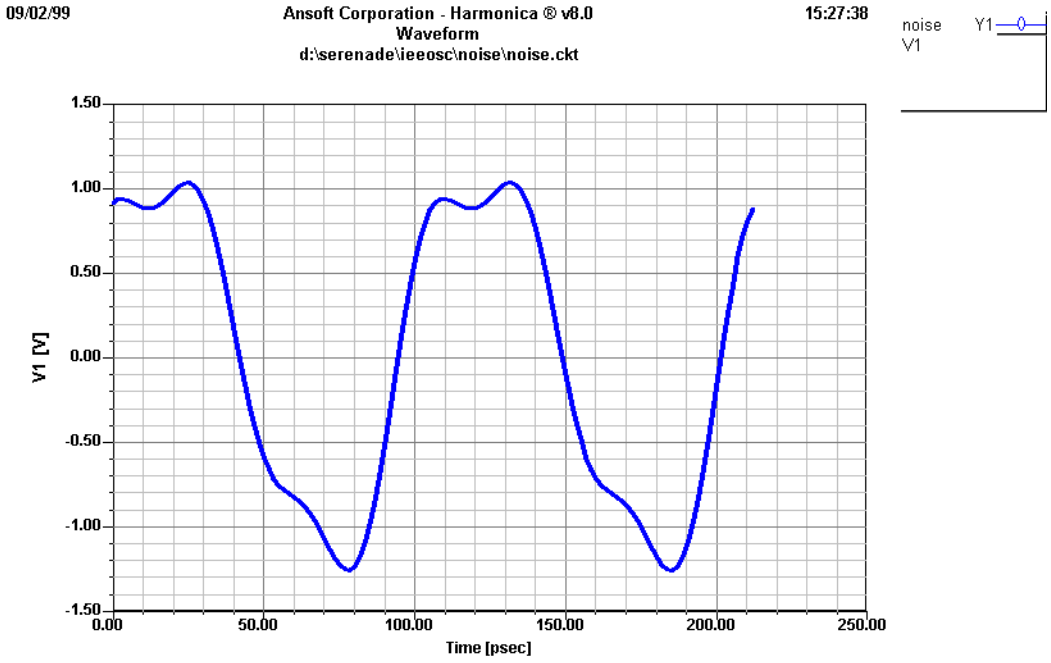

Figure 6: Oscillator Output Waveform

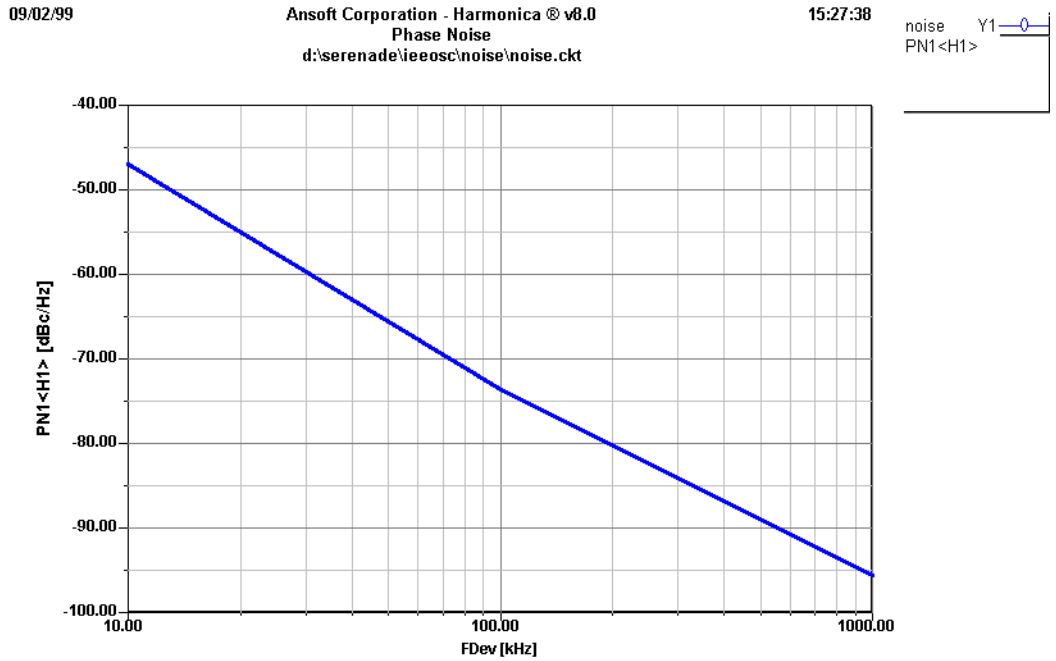

Figure 7: Prediction of Oscillator Phase Noise

Examples

This oscillator has been incorporated (in tuneable form) into the P35-4800 9.17 to 9.56 GHz Search And Rescue Transponder (SART) MMIC fabricated at MMT, Caswell (Ref. 3). The oscillator was made voltage controllable by incorporating a varactor into the gate resonator circuit. It must be noted that the transmission lines connecting the various elements need to be modelled at these frequencies. Although compact and simple to use, the principal disadvantages of a monolithic FET based oscillator are;

i. The poor 1/f noise performance of the active device

ii. The low Q of the lumped element resonator

iii. The poor tuning sensitivity of the monolithic varactor

In this particular application the resulting oscillator performance was perfectly acceptable for the simple transponder circuit. However, in many modern digital communication systems the phase noise performance is often inadequate. A prime example of this is the PRISM II wireless LAN ASIC from Intersil (Formerly Harris) (Ref. 4). The single chip receiver includes most functions, except for the oscillator. A high Q/low phase noise off-chip phase locked source is required for optimum performance. An on-chip oscillator would also most likely be pulled in frequency, as the chip switches between transmit & receive. This is due to poor isolation, and common-lead inductance problems. (Ref. 5)

A compromise between the use of off and on-chip oscillators in complex multi-function MMICs is widely used in the DBS receiver IC commonly fabricated by several companies, including Anadigics (Ref. 6). In this case an on-chip 2-port negative resistance circuit is designed on the chip, and this is coupled to a high Q off-

chip dielectric resonator. This allows the best compromise between integration and phase noise performance. The resulting phase noise can be some 30 dB better than that of an on-chip resonator.

Conclusions

A relatively simple and low cost small-signal RF/Microwave simulator can be used to determine the approximate frequency of oscillation of a MMIC oscillator by solving the resonant frequency equation for a simple closed loop equivalent circuit, and ensuring adequate excess -R for start-up. The use of a non-linear simulator (and suitable non-linear model) more accurately predicts the steady-state frequency of oscillation. In this particular example the two answers differed by < 1%. The harmonic balance simulation gives much more valuable information such as DC bias information, output power, harmonic content and phase noise. However, the small-signal simulation such not be overlooked as problems with inadequate negative resistance levels and potential spurious oscillation frequencies can be readily observed.

References

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