A Monolithic, Dual Channel, DC to 20GHz SPDT

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Abstract: This paper describes the design and evaluation of a Single Pole Double Throw (SPDT) switch IC covering DC to 20GHz. Two SPDTs are realised on each die to give a dual channel part for use in systems where accurate gain and phase matching between channels is vital. The switch was fabricated on Triquint Semiconductor Texas' 0.25µm PHEMT process and has a measured insertion loss of less than 1dB to 10GHz and less than 1.6dB to 20GHz. The input and output return losses are greater than 14dB to 20GHz and the 1dB compression point is +27dBm.

Introduction

The primary application for the switch design was a dual channel receiver, requiring amplitude and phase matching between channels. For this reason two SPDTs were fabricated on each IC. The functionality of the IC is depicted in Figure 1. Although the two SPDTs switch together in this application, the facility for independent control of each has been included as it increases the versatility of the IC in terms of its suitability for re-use in other applications.

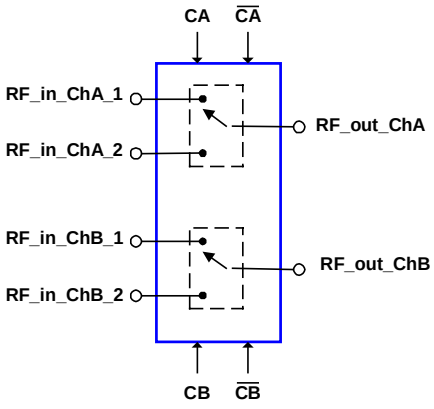

Figure 1: MMIC functionality

The IC process selected was the commercially available Triquint Semiconductor Texas' 0.25µm gate length Pseudomorphic High Electron Mobility Transistor (PHEMT) process. The suitability of PHEMTs for switch realisation stems from the fact that their drain-source resistance behaves as a voltage variable resistor, with the resistance value being set by the gate-source voltage [1]. When used as a switch, a PHEMT is operated with the drain and source at zero volts DC. The RF signal path is drain to source and the gate is the control terminal.

With depletion mode PHEMTs, such as those used, Vgs=0V results in a low resistance signal path (low Rds) and the transistor is on. For Vgs below pinch-off, the transistor has a high resistance signal path (high Rds) and the transistor is off.

The on-case resistance of transistors fabricated on the Triquint 0.25µm PHEMT process is around 1.8Ωmm and the off-case resistance about 10kΩmm. There is also a parasitic drain-source capacitance of around 0.3pF/mm. It is this capacitance that limits the high frequency isolation of the off-state transistor. This means that simple series/shunt switch topologies will not provide adequate performance to 20GHz [1] and alternative topologies need to be adopted, as described below.

Design

A distributed topology was adopted for the switch design, as shown in Figure 2. This technique extends the operating frequency of the switch by absorbing the off state capacitance of shunt mounted transistors into a low pass filter.

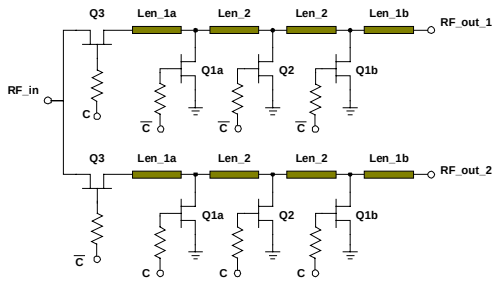

Figure 2: Schematic of the distributed SPDT

A length of high impedance transmission line, which represents the series inductance of the filter, separates each shunt transistor. Provided

the off-state capacitance of the transistors is low enough, a filter can be produced with a cut-off frequency beyond the desired upper operating frequency.

Table 1 shows the complementary switching control of the SPDT. The path from the input to one output is low loss whilst the path from the input to the other output is high isolation. The shunt mounted PHEMTs in the on-case path are pinched-off and the corresponding series device is switched on (low-resitance state). Since the parasitic capacitance of the shunt mounted transistors has been absorbed into a filter structure, the on-case path loss is low.

C	$\overline{C}$	Active output
0V	-5V	RF_out_1
-5V	0V	RF_out_2

Table 1: Truth table for the SPDT

The shunt mounted PHEMTs in the off-path are switched on and provide a low impedance path to ground. The corresponding series transistor is pinched-off and at low frequencies it is high impedance. At higher frequencies the parasitic capacitance means the transistor provides little isolation but the switch is designed so that the line length 1a and the series transistor transform the low impedance of the first shunt mounted transistor to a high impedance. Thus operation from DC to 20GHz is achieved with this structure.

The starting point for the design was to create a Low Pass Filter (LPF) with a cut-off frequency just above the desired upper operating frequency. A 7th order Tchebychev design [2] was used, as shown in Figure 3, which allows the absorption of 3 shunt transistors into the filter structure. The component values for this filter are given in Table 2.

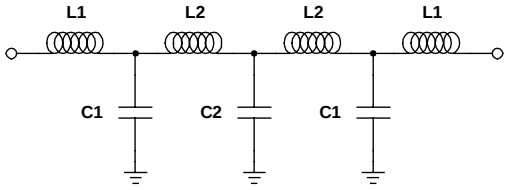

Figure 3: Schematic of the 23GHz LPF

Component	Value	Units
L1	0.291	nH
L2	0.637	nH
C1	0.203	pF
C2	0.238	pF

Table 2: LPF component values

Figure 4 is a plot of the simulated performance of the LPF, showing low insertion loss and high return loss from DC to 23GHz.

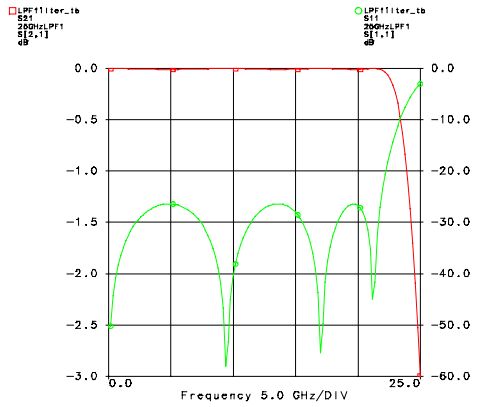

Figure 4: Simulated performance of LPF

The next step was to replace the shunt capacitors with transistors (Figure 5). Transistors of the appropriate size (gate width) were selected, such that their parasitic off-state capacitance is equal to that of the capacitor they are replacing. Thus with the transistors pinched-off, this structure has low insertion loss up to the cut-off frequency of the filter.

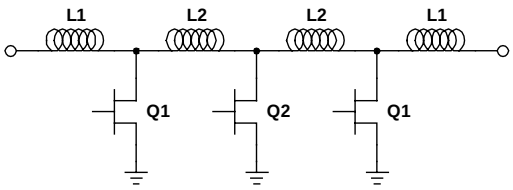

Figure 5: Schematic of LPF with capacitors replaced by PHEMTs

The simulated performance of the LPF after substituting the capacitors for transistors is shown in Figure 6. Low loss and good return loss is still achieved to 23GHz.

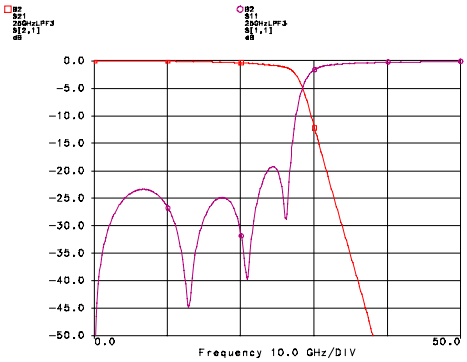

Figure 6: Simulated performance of LPF , capacitors replaced by off-state PHEMTs

The next step in the design process was to replace the ideal series inductors with lengths of high impedance, microstrip transmission line, as depicted in Figure 7.

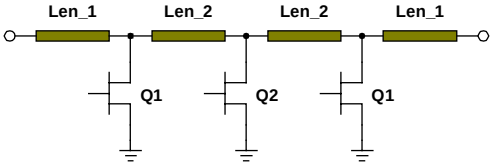

Figure 7: Schematic of LPF, using PHEMTs and microstrip line

The lengths of high impedance transmission line approximate the series inductive elements required by the low pass filter. The narrower the width of the microstrip line, the higher its characteristic impedance and the higher the inductance per unit length. The line lengths were optimised to give the simulated performance shown in Figure 8. The return loss is greater than 21dB (< 1.2:1 VSWR) from DC to 23GHz. With the transistors on (switch branch off), their low impedance results in the filter structure having a loss (isolation) in excess of 30dB.

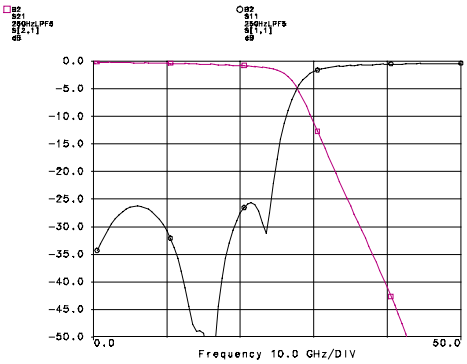

Figure 8: Simulated performance of the LPF of PHEMTs and microstrip line

The next stage of the design was to include a series PHEMT before the filter and to include both switch paths (on-case and off-case) in the simulation, so forming the complete SPDT circuit shown in Figure 2. The combination of series switching transistor and low pass filter must be well matched and have low insertion loss in the on-case (series transistors "on", shunt transistors "off") and a high insertion loss and a high input impedance in the off-case (series transistors "off", shunt transistors "on"). The fact that the off-branch of the SPDT has a high input impedance means that the inputs of the two branches can simply be commoned to form the complete SPDT.

The effects of the RF port bondwire inductance were also introduced into the simulation and the switch performance was re-optimised to account for this.

Choosing the size of the series transistors (Q3 in Figure 2) is a trade-off between better isolation but lower P-1dB and higher insertion loss (smaller device) or degraded isolation but improved P-1dB and reduced insertion loss (larger device). A 270µm gate width device was selected. The final simulated performance of the complete SPDT is shown in Figure 9. This includes all appropriate discontinuity and proximity effects of the IC layout and the bonding parasitics.

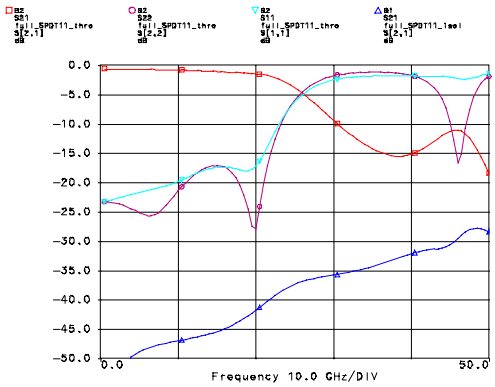

Figure 9: Final simulated performance of one SPDT

Realisation and Measured Performance

A photograph of the switch IC is shown in Figure 10, the die size is 1.525mm x 2.54mm.

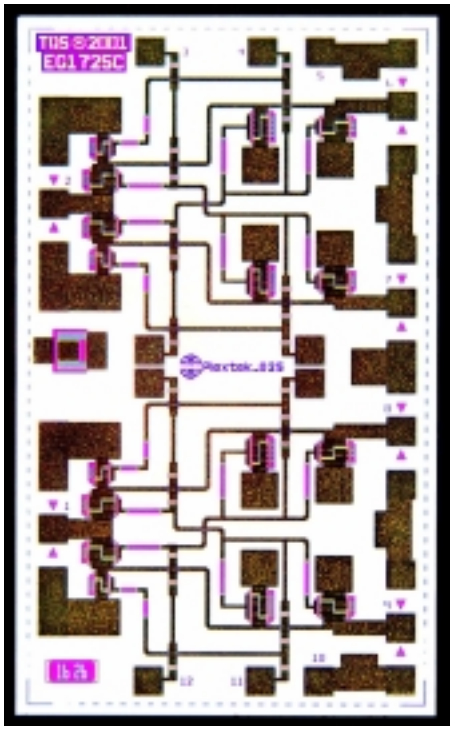

Figure 10: Photograph of the IC

Evaluation of the switch was carried out on ICs assembled onto an MIC carrier tile, as shown in Figure 11. This was fabricated from 0.01"

thick RT/Duroid 5880 with a brass backing to give rigidity. The small size of the die means the RF input/output lines are closely spaced. Using a thinner substrate would have resulted in thinner lines and eased this problem.

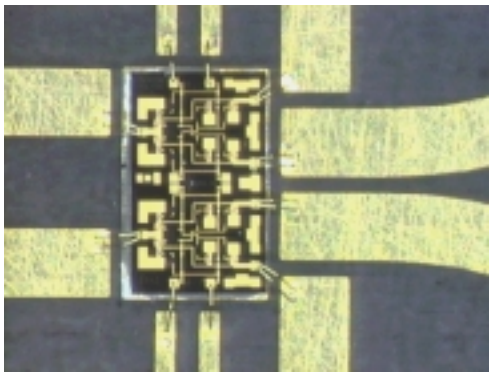

Figure 11: Photograph of an IC assembled onto a carrier

A comparison of the measured versus modelled insertion loss and return loss is shown in Figure 12. Good agreement has been obtained across the entire band. The insertion loss is less than 1dB to 10GHz and less than 1.6dB to 20GHz. The input and output return losses are greater than 14dB to 20GHz

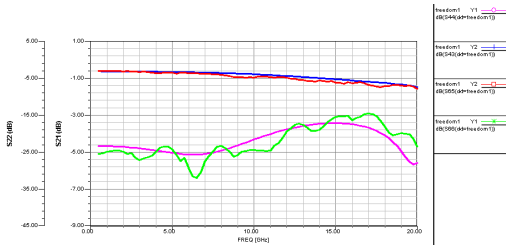

Figure 12: Measured versus modelled match and insertion loss

The measured isolation is shown in Figure 13 and is better than 22dB to 20GHz. This is poorer than the simulated isolation but this is almost certainly a result of coupling between the close proximity RF feed lines on the carrier substrate.

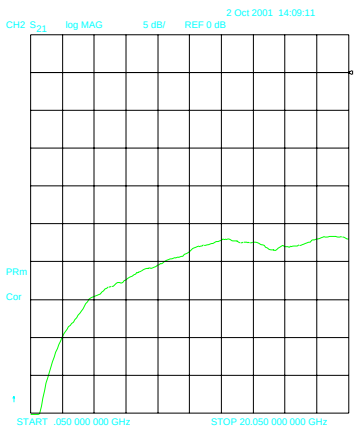

Figure 13: Measured isolation

The power transfer characteristics of the switch have also been measured. Figure 14 shows the insertion loss versus input power at 4GHz. For control voltages of 0/-5V the 1dB compression point is +27dBm and slightly higher with control voltages of 0/-8V.

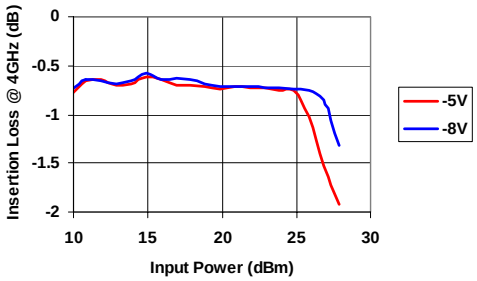

Figure 14: Measured insertion loss versus input power at 4GHz

Summary

A dual channel DC-20GHz SPDT has been designed, fabricated and evaluated. The die size is 1.525mm x 2.54mm. Evaluation was carried out on die assembled onto an MIC carrier. A summary of the measured performance is given below:

- Insertion loss below 5GHz < 0.7dB
- Insertion loss below 10GHz < 1dB
- Insertion loss below 20GHz < 1.6dB
- Return loss > 14dB to 20GHz
- Isolation > 22dB to 20GHz
- P-1dB +27dBm (-5V control)

The realisation of two SPDTs, on to a single die, offers benefits for use in dual channel systems where accurate amplitude and phase matching between channels is required.

References

[1] Liam Devlin, "The Design of Integrated Switches and Phase Shifters", Proceedings of the IEE Tutorial Colloquium on "Design of RFICs and MMICs", Wednesday 24th November 1999, pp 2/1-14

[2] Matthaei, Young and Jones, "Microwave Filters, Impedance-Matching Networks and Coupling Structures", Artech House 1980, ISBN 0-89006-099-1