A Low Cost V-band Amplifier MMIC Covering 54 to 67GHz

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Abstract

This paper describes the design and measured performance of a low cost amplifier MMIC covering 54 to 67GHz. The IC is realised on a low cost GaAs PHEMT process produced on 6" diameter wafers with optically defined gates. The two stage design operates from a single +3V supply (44mA) with a gain of 11.5dB. The measured 1dB gain compressed output power level is +12dBm. The design includes self bias resistors to reduce performance variation with process and temperature. The paper includes details of the design approach, the simulated performance, including EM, and the RFOW measured performance.

Introduction

Large amounts of spectrum at around 60GHz are now available on an unlicensed basis in many countries around the world [1]. This has generated interest from a wide range of potential applications including WLAN, WPAN and point to point links. The largest allocation of 60GHz spectrum is in the US where 7GHz is available (from 57 to 64GHz) without any channelisation requirements.

The purpose of the development described in this paper was to realise a low cost amplifier covering the full 57 to 64GHz band with reasonable gain and useful output power. A two stage design was developed on a low cost GaAs PHEMT process, available on a commercial foundry basis through TriQuint Semiconductor. The process features optically defined 0.13µm gates and is fabricated on 6" (150mm) diameter wafers. Operation from a single +3V supply was also desirable and this feature was included in the design.

Design

At high mm-wave frequencies the available gain of transistors drops as device size (unit width and number of fingers) increases. Achieving a reasonable output power level and adequate gain is a challenge [2]. Operation from a single positive supply further exacerbates this problem. Single supply operation of depletion mode HEMTs requires the source to be floated bypassing the drain-source bias current (Ids) through a resistor. This resistor is bypassed with a capacitor to provide a low impedance RF path. However, at mm-wave frequencies the parasitic inductances associated with the by-pass capacitor can start to have a significant effect on the RF performance.

Figure 1 is a layout plot of a 6x20µm transistor including the self bias resistors and bypass capacitors. The capacitor length is kept short to keep the effective inductance low and provide a better RF path to ground at 60GHz. This was the device size used for the output stage with a smaller, 4x16µm, device selected for the input stage. Test-pieces were fabricated comprising the two different transistors each with self-bias resistors and bypass capacitors. These were then measured to provide accurate data for the design.

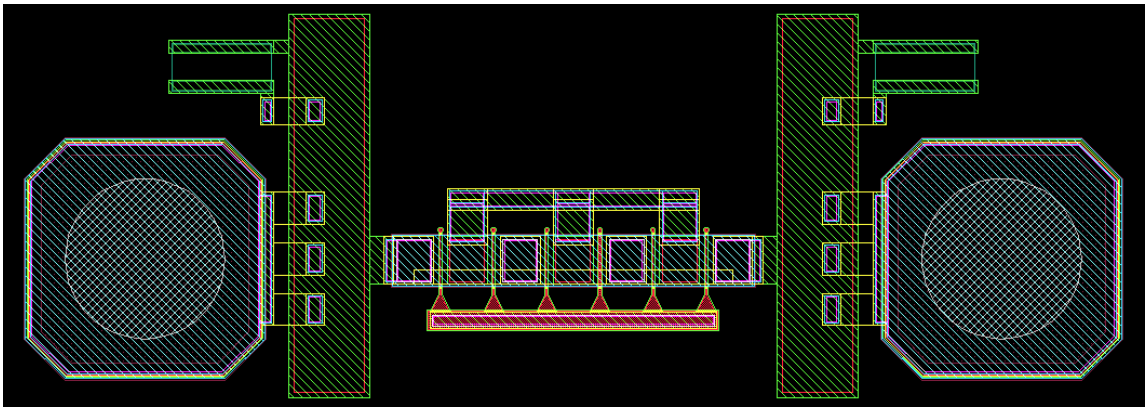

Figure 1: Layout plot of the output transistor with self biasing arrangement

The transistor test pieces were measured with the reference planes set at the gate and drain pads. The TQP13 process is actually a semi-enhancement process and a small positive gate-source voltage is required to set the correct transistor bias. The self bias resistors increase the value of the required gate voltage, which is set via a potential divider in the full amplifier. The inclusion of self-bias source resistors helps to stabilise the bias point and should also lead to reduced performance variation with temperature.

The MAG (Maximum Available Gain) versus frequency generated from the measured s-parameters of each of the transistor test pieces, including the self-bias resistors and by-pass capacitors, is plotted in Figure 2. The red trace is the stage 1 transistor and the blue trace the stage 2 transistor. It can be seen that at 60GHz the transistors have around 7 to 8dB of available gain. The stage 1 transistor is unconditionally stable from around 55 to 80GHz, i.e. across the entire band of interest. This can also be seen in the stability plot of Figure 3. The stage 2 transistor has a k-factor very close to 1 across the same frequency range.

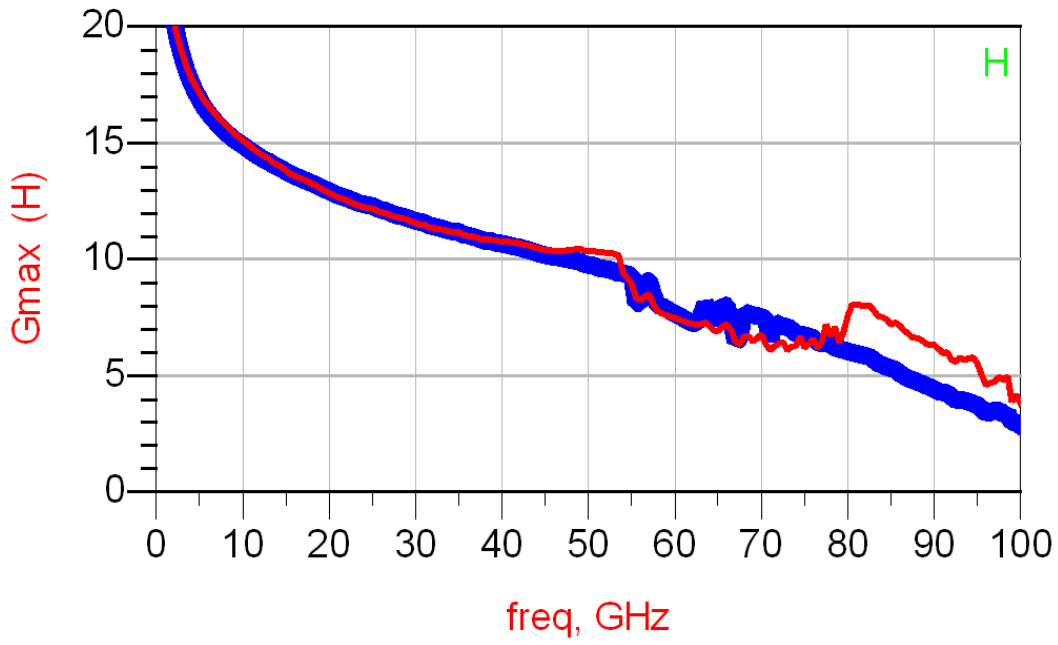

Figure 2: Measured Gmax versus frequency of stage 1 and stage 2 transistors with self bias network

The self-bias configuration (by-pass capacitance and associated interconnect tracking) of the two transistors was selected to stabilize them over the planned operating band. If the transistors were not

unconditionally stable then gain would need to be sacrificed to provide in-band stability. Ensuring stability above and below the operating band, which is also necessary, can be undertaken with frequency selective circuitry which has less of an impact on in-band gain. This approach was found to be the most effective way of ensuring in-band stability whilst minimizing the reduction in available gain.

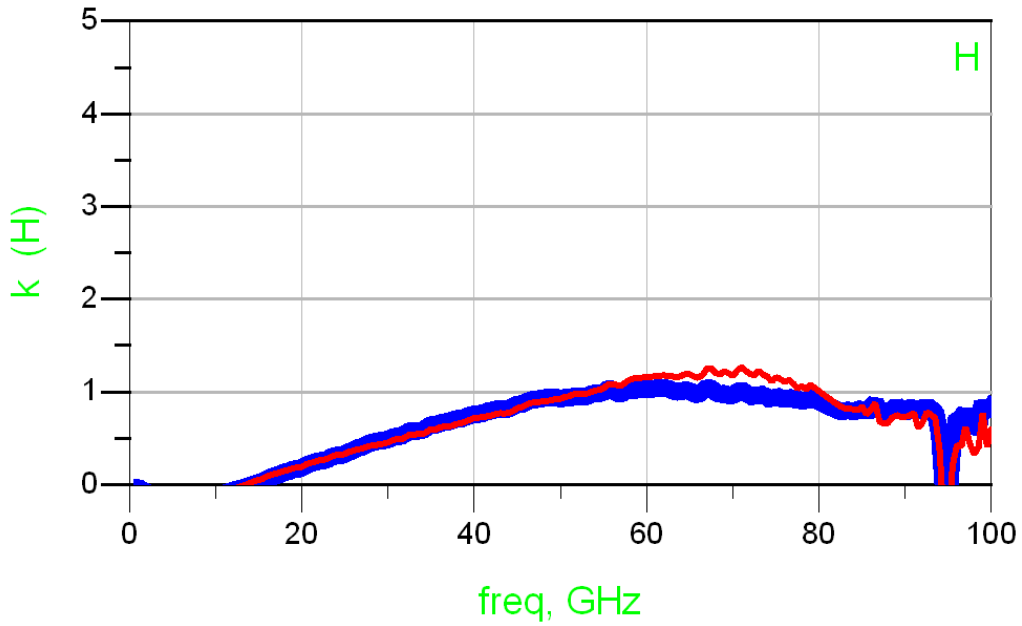

Figure 3: Measured K factor versus frequency of stage 1 and stage 2 transistors with self bias network

The maximum available gain of the two self-biased transistors is around 7 to 8dB in the band of interest. If reasonable gain is to be provided from the complete two stage design there is not much scope for incurring losses. Much of the effort during the design process was therefore devoted to limiting the reduction in available gain due to practical implementation details (matching networks, biasing networks and circuitry to ensure stability above and below the operating band). Figure 4 shows a simplified schematic of the biasing network used for each transistor. It includes components to ensure stability below the operating band where the transistors have a large amount of available gain.

RSB and CSB are the self bias components discussed above. In reality parallel copies of this network are included on each side of the transistor (as shown in Figure 1) to reduce grounding inductance and maintain symmetry. Gate and drain bias is injected through transmission lines TL1 and TL2. The remote end of the transmission line (the bias injection point) is grounded through a capacitor CRF. The dimensions of the capacitor were selected to provide a good in-band short-circuit and the lengths of TL1 and TL2 were then adjusted to transform this short-circuit to an open circuit at the transistor.

At lower frequencies, well below band, the capacitor CRF is not large enough to provide a good short-circuit. This provides an opportunity to introduce stabilizing resistors RGB and RGD, which are connected to ground through capacitors CGB and CGD. These are on-chip capacitors but are much larger than CRF and provide good low impedance paths down to below 1GHz. Off-chip de-coupling can be used to assist with ensuring stability at frequencies below this. Low cost SMT capacitors can be used for this purpose and more expensive microwave Single Layer Capacitors (SLCs) are not required.

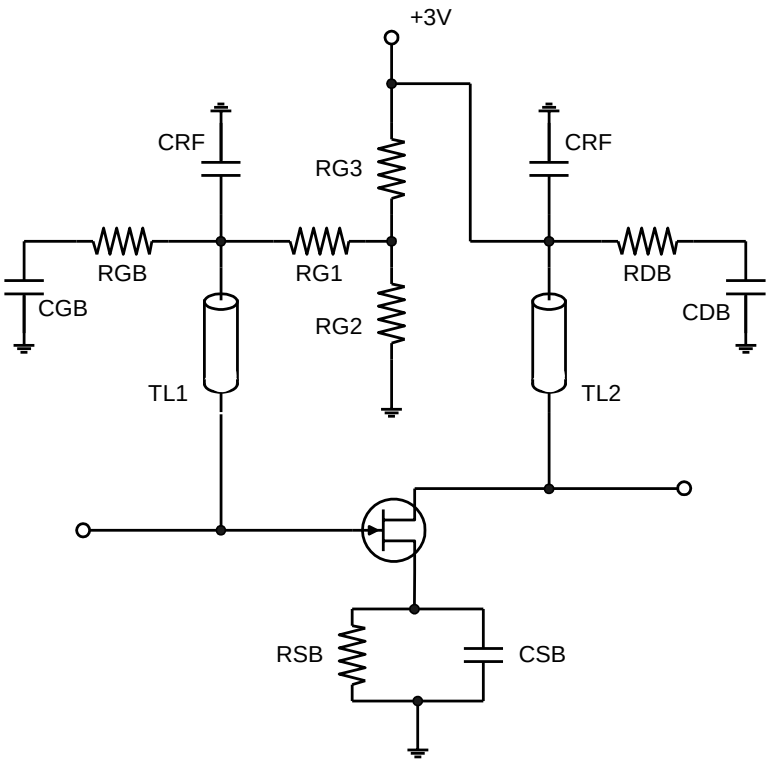

Figure 4: Simplified schematic of transistor biasing and low frequency stabilising network

The next step in the design process was to implement the matching networks. Low-pass distributed structures comprising narrow series transmission lines and open-circuit stubs were used for this purpose. Short-circuit stubs were also introduced as a means of further improving low frequency stability. Some modest resistive elements were introduced into the gate bias stubs to provide frequency selective loss and flatten the gain versus frequency response. These elements are all evident from inspection of the layout plot in Figure 5.

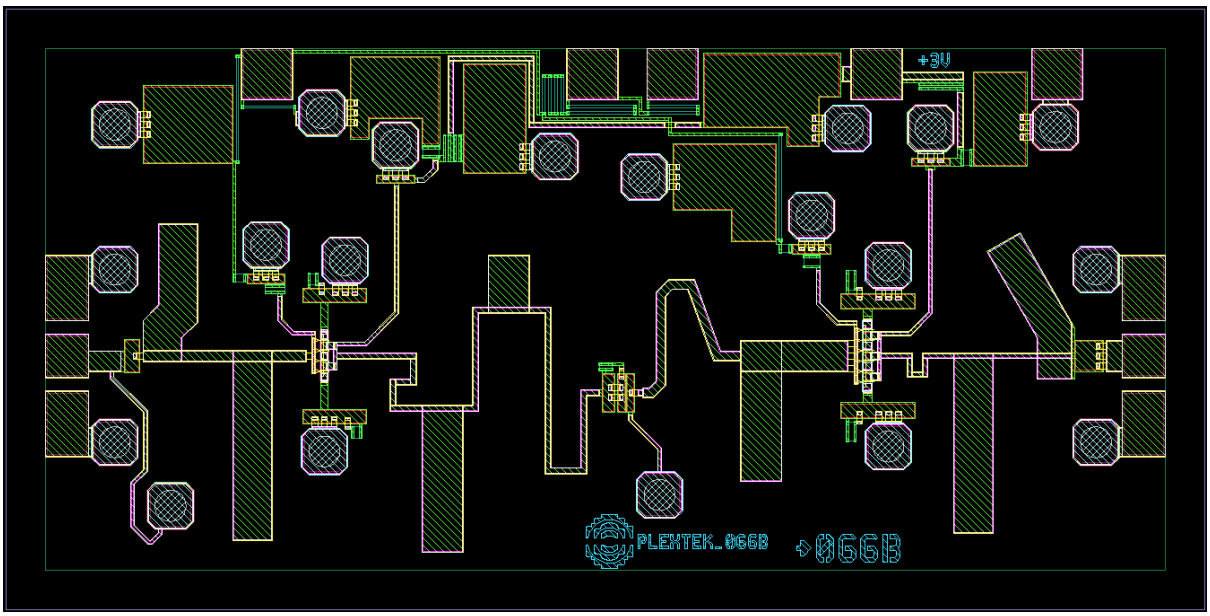

Figure 5: Layout of the 60GHz amplifier

One of the key difficulties throughout the design process was in ensuring that the accumulated losses incurred in the practical implementation did not excessively degrade the gain. As previously mentioned the design was based on measured s-parameters of the self-biased transistor test pieces. In the first instance the passive components (transmission lines, capacitors, resistors and vias) were simulated using the models from the Process Design Kit (PDK)). The performance of the design was optimized and a first-pass of the amplifier layout was produced.

The next stage in the design process was to EM simulate the metalwork and re-optimise the design and layout to compensate for the discontinuity and proximity effects that became evident. This process was completed step by step with increasing amounts of the circuit gradually EM simulated. Careful re-optimisation was undertaken at each stage to try to avoid reducing the amplifier's gain and to maintain good input and output return losses. The simulated s-parameters of the final circuit including EM are plotted in Figure 6. The gain is around 11dB from 56 to 66GHz with input return loss better than 15dB and output return loss better than 14dB.

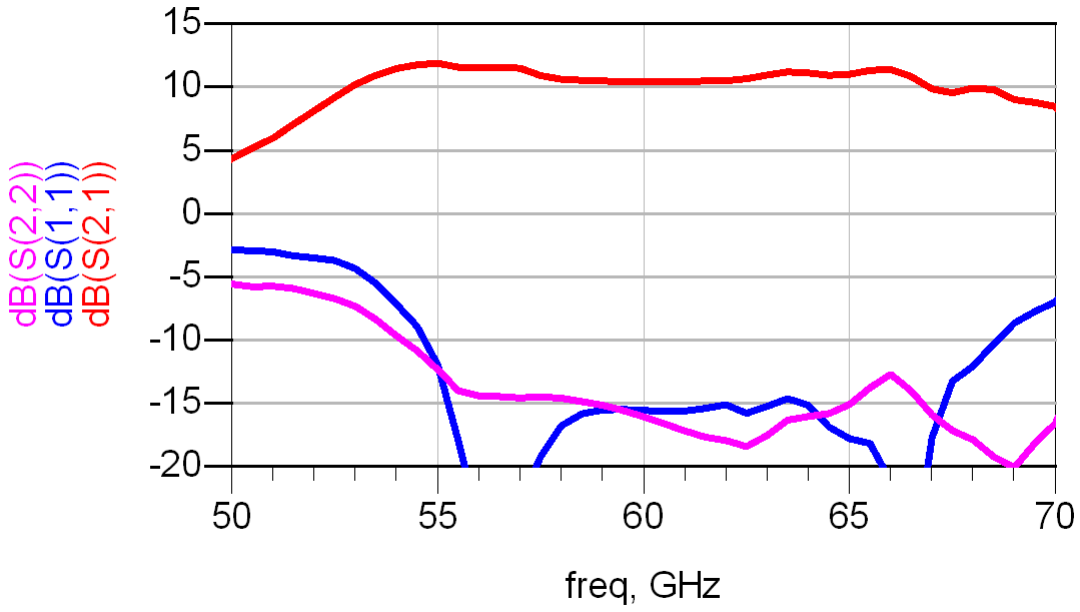

Figure 6: Simulated s-parameters of final design including EM

As the design was based on measured s-parameter data, the large signal performance could not be directly simulated. However, the estimated P-1dB was +13dBm, which is slightly higher than that measured (see below).

In any amplifier design it is vital to ensure that the amplifier is unconditionally stable across the full range of frequencies where the transistors have available gain and therefore the potential to cause instability. Particular care must be taken at low frequencies where short gate length transistors have very large amounts of available gain.

Fabrication and Measured Performance

A photograph of one of the amplifier die is shown in Figure 7. It can be seen that the y-dimension is larger than required. This was to allow arraying of the IC on a multi-project mask set. The production version of the die will have a reduced Y-dimension.

The amplifier operates from a single +3V supply (±10%). There are two bondable options for connecting the gate supply:

- Bias#1 bonded to Vdd (Ids ≈ 44mA)
- Bias#2 bonded to Vdd (Ids ≈ 53mA)

It was originally intended that bias #2 could provide a means of providing a modest improvement in P-1dB. However measurements revealed that both small signal and large signal performance is very similar for both bias modes and so bias #1 is preferred for its lower current operation.

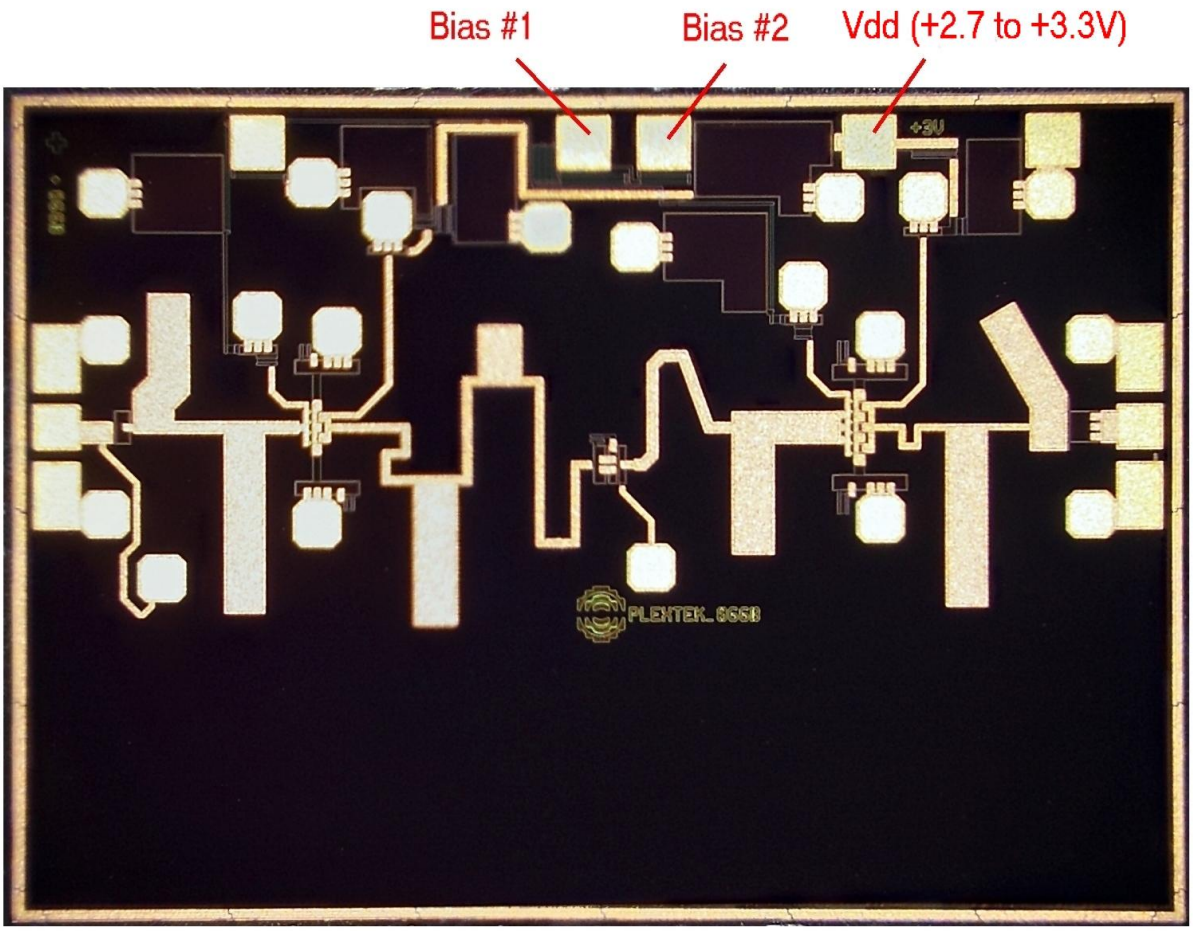

Figure 7: Photograph of the 60GHz amplifier

The RFOW measured s-parameters of a typical amplifier are plotted in Figure 8. Calibration to the probe tips using an Impedance Standard Substrate (ISS) was used [3]. Two traces are shown, the red trace is for bias #1 (Ids = 44mA) and the blue trace for bias #2 (Idd = 53mA). There is very little difference in the small signal performance. Across the US ISM band of 57 to 64GHz the gain is 11.5dB ±0.5dB. Across the wider band of 54 to 67GHz gain variation increases slightly but input return loss remains better than 6dB and output return loss better than 10dB.

The performance variation with drain supply voltage (for bias#2) is plotted in Figure 9. There is very little difference in small signal performance for a ±10% variation in supply.

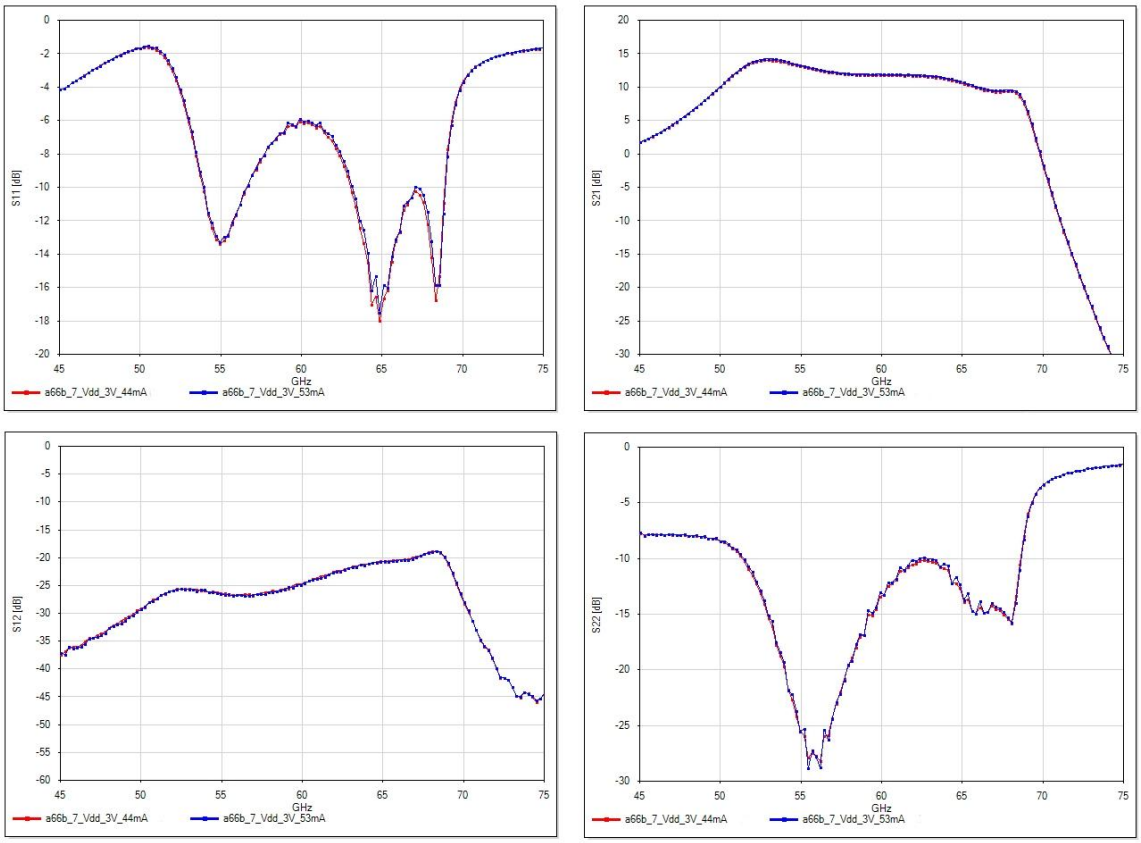

Figure 8: Measured s-parameters at Vdd = 3V for bias #1 and bias #2

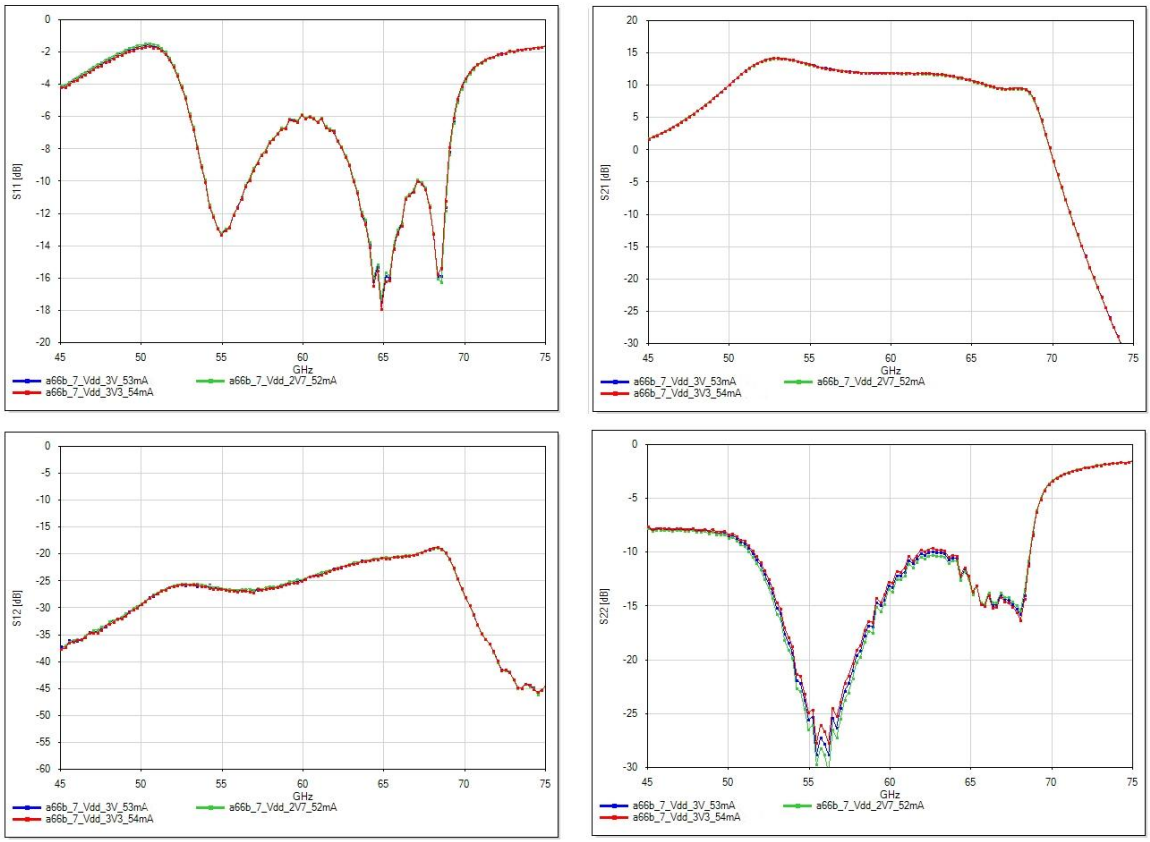

Figure 9: Measured s-parameters for supply voltages of 2.7V, 3V and 3.3V (bias #2)

The measured power transfer characteristics at 60GHz for a +3V supply are shown in Figure 10. This measurement was for bias #1, power transfer measurements were also undertaken at bias #2 but no improvement in compression performance was evident. Measurements were also undertaken at 54GHz and 67GHz and showed similar P-1dB performance.

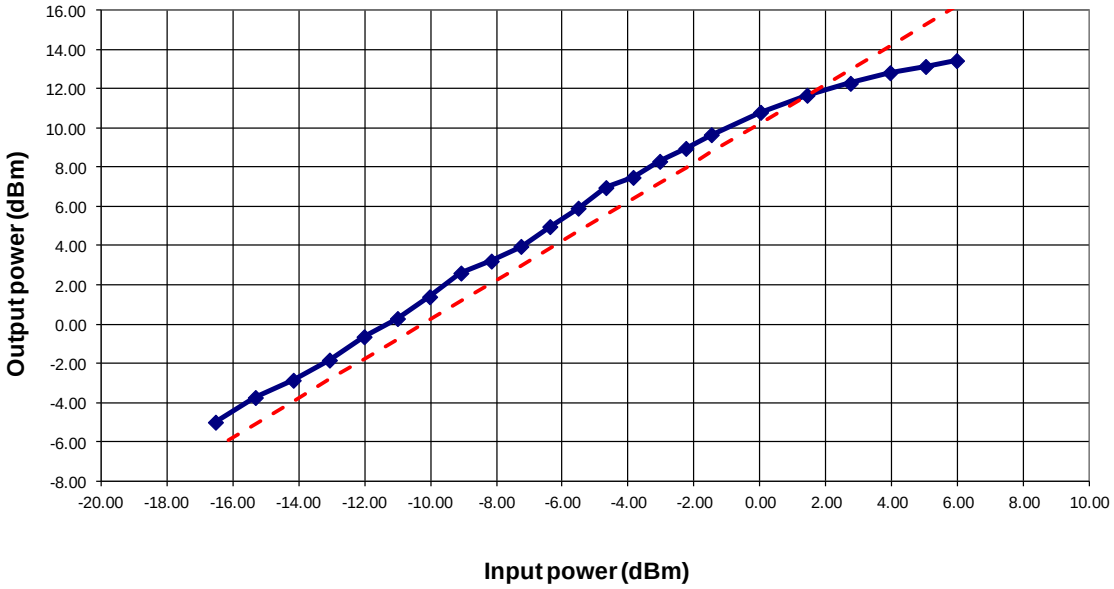

Figure 10: Measured power transfer characteristics at 60GHz (3V Vdd, bias #1)

Conclusions and Summary

This paper has presented the design, simulation and measured performance of a low-cost two stage amplifier covering 54 to 67GHz. The amplifier operates from a single +3V supply with a quiescent current of 44mA. It provides a gain of 11.5dB and an output power (at P-1dB) of +12dBm. A summary of the measured performance is presented in Table 1.

Parameter	Value	Units
Frequency range	54-67	GHz
Gain	11.6 ± 2.2	dB
Gain (57-64GHz)	11.6 ± 0.5	dB
Input return loss	>6	dB
Output return loss	>10	dB
P-1dB	12	dBm
Supply current (Bias 1) for Vdd=3V±0.3V	~44	mA
Supply current (Bias 2) for Vdd=3V±0.3V	~53	mA

Table 1: Performance summary

References

[1] J.A. Wells, "Multi-Gigabit Microwave and Millimeter-Wave Wireless Communications," Boston, Artech House, 2010

[2] Liam Devlin, Stuart Glynn, Graham Pearson, Andy Dearn, "The Design of E-band MMIC Amplifiers", proceedings of the RF and Microwave Society (ARMMS) Conference, April 19th and 10th, 2010

[3] Graham Pearson, "RFOW calibration using a Cascade Microtech ISS", Technical Tutorial Video from Plextek RFI: http://www.youtube.com/watch?v=EYEXf9miflQ