Designing Digitally Tunable Microwave Filter MMICs

Tunable filters are a vital component in broadband receivers and transmitters for defence and test/measurement applications. The very low component parasitics that can be achieved on an MMIC (Microwave Monolihic Integrated Circuit) allow the reailsation of compact, low-cost tunable microwave filters. This technical briefing discusses the design, realisation and achievable performance of digitally tunable filter MMICs.

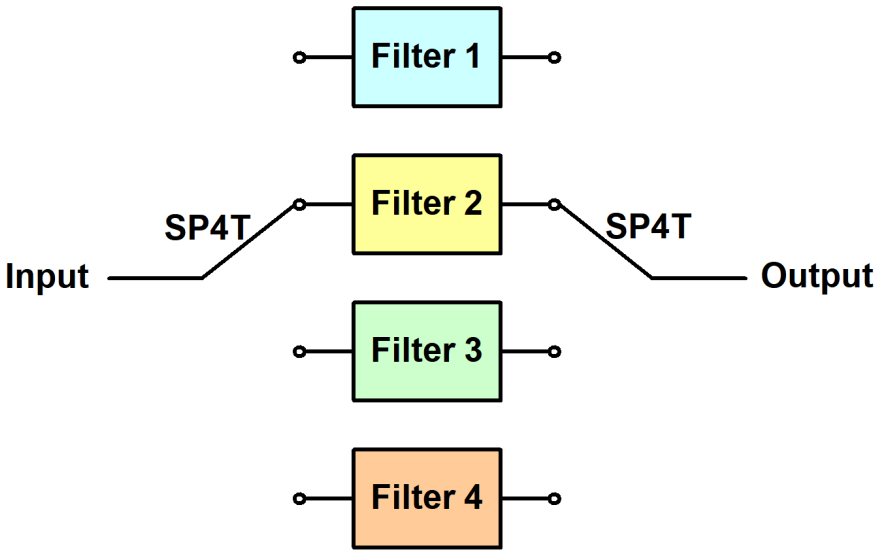

Figure 1: Switched filter bank

Commercially available GaAs MMIC processes allow the realisation of components that can be used to implement passive filters, these include:

- Capacitors, usually in the form of a Metal-Insulator-Metal (MIM) sandwich
- Inductors, typically wound spirally on the MMIC surface using one or more metallisation layers
- Distributed elements such as:
  - Transmission lines, typically electrically short (<λ/10) lengths of metallisation used to form small inductances
  - Coupled lines in the form of comb lines, interdigital lines and parallel coupled lines

These components can be combined to form useful filtering responses such as low pass, band pass, high pass and band stop functions.

The simplest form of digitally controlled filter that could be realised on an MMIC is a switched filter bank as depicted in Figure 1. Here four separate filter functions have been designed and one of the four is selected at any one instance. Two single pole four throw (SP4T) switches are used, one at the input and one at the output, to select the desired filter. The SP4Ts are usually realised using depletion mode FETs that are available on the MMIC process. Here the FETs are biased in their linear region with Vds = 0V and Vgs =0V to obtain a low resistance 'ON' state, and with Vds = 0V and Vgs < 0V (typically -2V to -5V for modern MMIC processes) to obtain a high resistance 'OFF' state. With appropriate design techniques the circuit can be configured such that it operates from positive logic, and a negative voltage is not required.

The downsides to the simple switched filter bank approach are size (die area) and the fact that only a modest number of selectable filters can be used. Rather than create four separate filters as depicted in Figure 1, an alternative

Plextek RFI Ltd. The Plextek Building, London Road, Great Chesterford, Saffron Walden, CB10 1NY, UK

T: +44 (0) 1799 533200 **E:** enquiries@plextekrfi.com **W:** www.plextekrfi.com

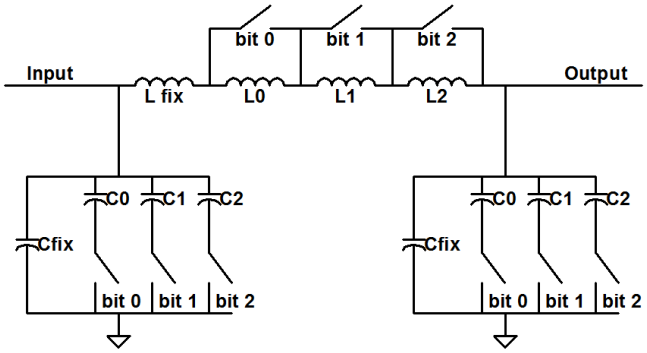

Figure 2: : Example of a 3-bit tunable low pass filter

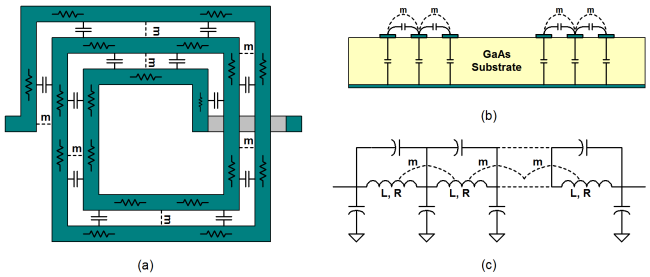

Figure 3: MMIC spiral inductor depicting the dominant parasitic elements at microwave frequencies. a) view from above, b) cross section, c) equivalent circuit

approach would be to implement a reconfigurable filter. With this approach, one common filter structure is used but individual components within the filter are switched to tune its response across a broad range of frequencies; this approach leads to a design with a much reduced die area.

Figure 2 depicts a digitally tunable reconfigurable Low Pass Filter (LPF). In this example a three section low pass filter in Pi format has been created using lumped elements comprising a series inductor and two shunt capacitors. The inductor element comprises four inductors and three switches to make it 3-bit tunable. The shunt capacitor elements comprise four capacitors and three switches to also make it 3-bit tunable. If the individual inductors and capacitors are binary weighted then appropriate selection of the bit switches can allow a range of low pass responses to be created.

The filter implementation of Figure 2 has the disadvantage that the low value series inductors in typical RF filters require very low loss, very low parasitic switches in order to maintain an acceptable filter response – lower than can be achieved in practise. Fortunately it is possible to develop Low Pass, Band Pass and Band Stop filters that need only make use of switched capacitors, which simplifies the control requirements, reduces implementation complexity and allows for lower insertion loss. This is the approach that will be described below.

The MIM capacitors implemented on GaAs MMIC process have good accuracy and relatively high Q (low loss) and it is the inductor and switch losses that are the dominant contributors to the overall filter loss. Figure 3 depicts the dominant parasitic elements of a spiral inductor. The mutual inductance 'm' between adjacent tracks increases the overall inductance and is the reason for adopting the spiral topology. The inter track capacitance, the capacitance between a track and ground and the resistive losses in the tracks are undesirable parasitics that must be accomodated in the design process.

Determining the correct dimensions of the spiral inductor to achieve a particular inductance is accompanied by trade-offs which must be taken into account when operating at microwave frequencies. For example, to achieve the highest Q inductor, one would expect that having wide tracks would reduce the series resistance. However, wide tracks also reduce the series inductance, so to counter for the reduction in inductance, one might reduce the separation between tracks to increase the coil's mutual inductance. Moving tracks closer increases the inter track capacitance and using wider tracks increases the capacitance between track and ground. Together these two parasitics work to reduce the coil's parallel resonant frequency and therefore the useful frequency range over which the coil appears inductive. Making the coil tracks too wide and too closely spaced can result in a component where the parallel self resonant frequency is within the frequency range of the filter and therefore cause it to appear inductive below resonance and capacitive above resonance; clearly an

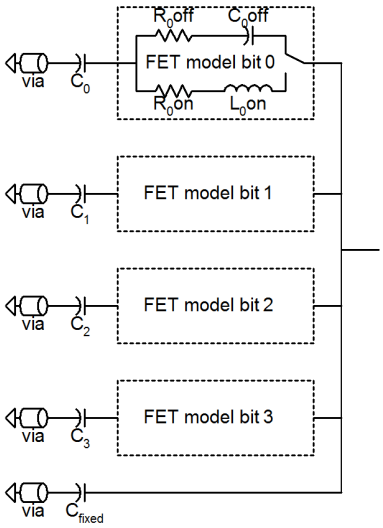

Figure 4: A four bit switched capacitor bank schematic showing FET

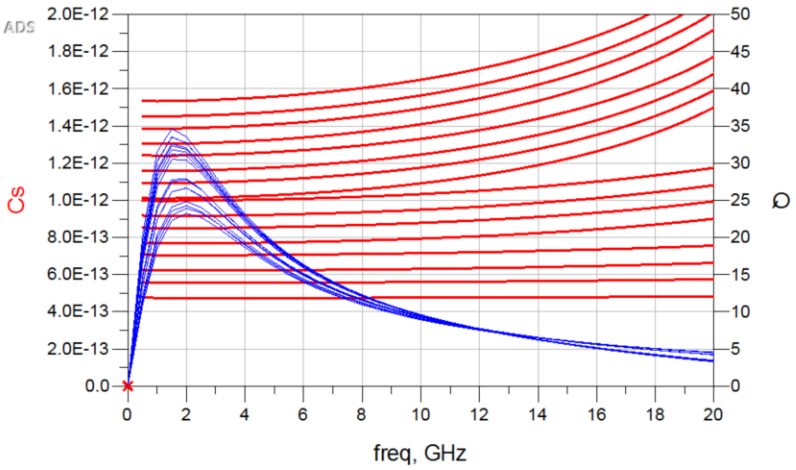

Figure 5: Capacitance and Q of the 4-bit switched capacitor bank optimised for 12GHz operation

undesirable property that must be avoided. Consequently an iterative design process takes place when determining the correct size of MMIC inductors for an application in a particular frequency range.

The binary weighted capacitors depicted in Figure 2 comprise series combinations of MIM capacitors and FET switches paralleled together. A single fixed MIM capacitor, also in parallel, can be added to set an overall capacitive offset to the bank.

Whilst one might expect capacitors to be ratioed in a 1-2-4-8-… manner in a design for a low frequency binary weighted application, the same approach does not work at RF. At RF frequencies, the parasitic impedances of each FET switch in both 'ON' and 'OFF' state affect the overall tuning range of the resulting bank and must be taken into account in the design process. Consequently both FET size (number of gate fingers and gate width) and capacitor area for each series branch need to be individually optimised to obtain the desired capacitance tuning range and Q. As a consequence, modelling and optimising the FET switches and MIM capacitors in the target IC process is a vital part of the design cycle.

Figure 4 depicts the schematic of a four-bit capacitor bank with each FET switch individually modelled in both 'OFF' and 'ON' state by appropriate parasitic elements.

Figure 5 shows the capacitance and Q of the 16 states of the switched capacitor bank optimised, in this case, to be centred on 1.1pF with a constant Q at 12GHz. In this example, the capacitor bank Q is 7.5 – a figure significantly lower than the Q of an individual MIM capacitor (typically >200 at 12GHz). The cause of this Q degradation is the resistive losses within the FET switches.

The design of a tunable RF bandpass filter begins with a low pass prototype filter with the desired characteristics that is then scaled in impedance and frequency and transformed into a bandpass topology. Figure 6 depicts a 3rd order bandpass filter following such transformations; this example is centred on 12GHz with a 2.8GHz bandwidth. Tuning this topology using the capacitor bank architecture of Figure 4 is problematic: whilst the two shunt 1.14pF capacitors are well matched to the capacitor bank realisation, the series 31fF capacitor, which must also be tuned, is tiny in proportion and too small to be suited to a FET switched binary weighted capacitor.

The problem encountered in Figure 6 is conveniently overcome by transforming the bandpass filter into a coupled resonator form as depicted in Figure 7. In this transform, all capacitive tuning elements have the same (1.14pF) value and all are referenced to ground. It is now possible to replace each fixed capacitor with the same capacitor bank structure and gang the control bits together to obtain a tunable filter practical for MMIC realisation. The fact that each capacitor bank is identical to the others means the filter topology is well suited to tracking with frequency.

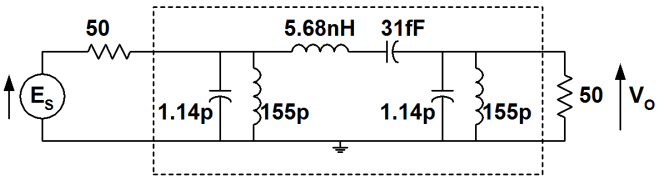

Figure 6: Bandpass filter centred on 12GHz with a 2.8GHz bandwidth

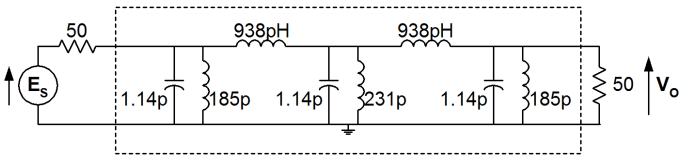

Figure 7: Bandpass filter of Figure 6 transformed into coupled resonator form

The coupled resonator bandpass filter has been simulated with practical models for all components, and the shunt capacitor implemented as binary weighted switched capacitor banks. The frequency response for the 16 different states of the tunable filter is plotted in Figure 8.

The FET switch and MIM capacitor dimensions for each bit branch of the switched capacitor network must be individually optimised to obtain an even stepped frequency response and a near flat insertion loss. In this example, the filter tunes from 10GHz to 14.5GHz, has a bandwidth between 2 and 3GHz and an insertion loss of <9dB. An initial layout placement of the central switched coupled resonator part of the coupled bandpass filter of Figure 7 in the chosen process is depicted in Figure 9.

Similar switched capacitive tuning techniques can be used to realise RF low pass and RF high pass filters, again developed from familiar low pass prototype polynomial designs such as Butterworth, Chebyshev, Elliptic, Bessel and so on.

Realisation of tunable band stop filters is more challenging. The relatively low Q of tunable resonator structures results in limited notch depths at RF – typically between 15 and 30dB – and limited minimum bandwidths. As with band pass filters, it is possible to realise band stop filters in coupled resonator form but they have a limited upper frequency. In this case, the switched capacitor bank is applied as a series component rather than the shunt arrangement used for the band pass filter. It therefore has more parasitic elements to ground that impact the filter response.

An alternative approach is to develop a bandstop filter using a 90 degree hybrid and two band pass filters as depicted in Figure 10. Here the input signal enters the hybrid's 0 degree port and is split into two equal signals that leave the -90deg and -180deg ports. The two identical band pass filters absorb signals within the passband and reject signals outside the pass band by reflecting these back into the hybrid where they combine to form an output at the isolated port. Thus all those signals not absorbed by the band pass filters, i.e. the out-of-band signals, pass from input to output, whilst those that pass through the band pass filters dissipate in the terminaing loads. The transmission through the composite structure is therefore that of a band stop response. The shape of the band stop response is that of the reflection response of the band pass filter.

Figure 11 depicts the response and return loss of a band stop filter constructed using a 90 degree hybrid, realised as a Lange coupler on the MMIC, and two band pass filters. The filter has been optimised to tune from 10 to 15GHz, has a pass band insertion loss of between 1 and 2dB and a notch 3dB bandwidth between 3.5 and 5.5GHz. Notch depth is dependent on the Q of the filter elements and on frequency offset from centre frequency. The downside to this approach is the additional die area required compared to the tunable bandpass filter.

In summary, the very low component parasitics that can be achieved on a GaAs MMIC process allows the realisation of compact, low-cost tunable microwave filters. It is possible to generate useful low pass, high pass, band pass and band stop filter responses that are digitally tuned using switched capacitor banks providing care is taken to model the FET switches accurately and all parasitic elements are taken into account.

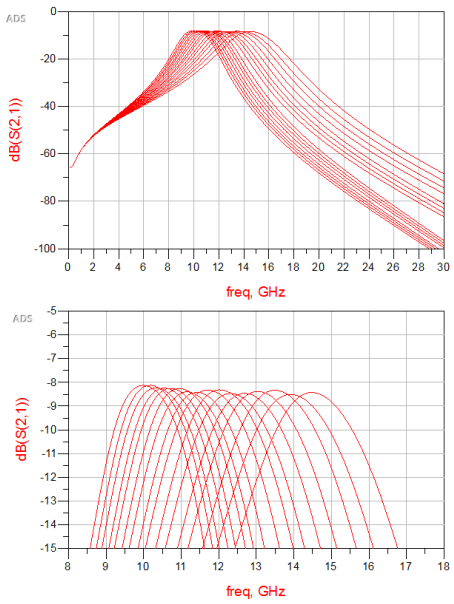

Figure 8: Frequency response and return loss of the coupled resonator filter with 4-bit tuning

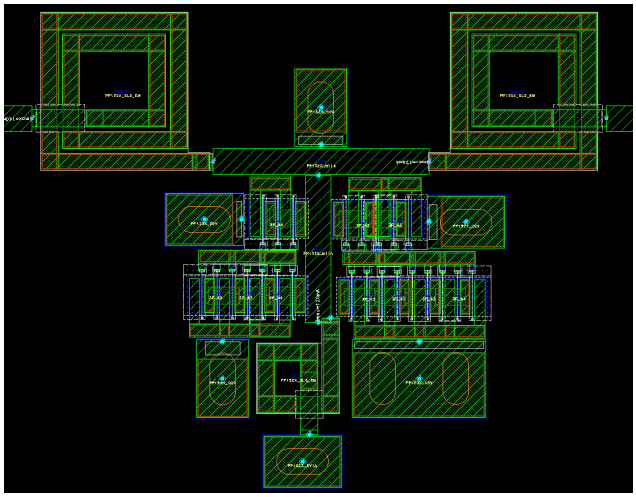

Figure 9: Layout placement of the central switched capacitor tuned resonator. Coupling inductors to the other resonators are visible at the top

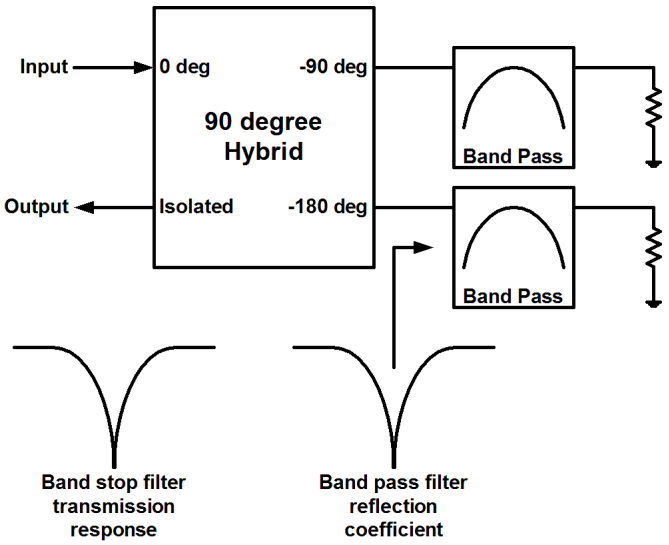

Figure 10: Band stop response created using a 90 degree hybrid and two bandpass filters.

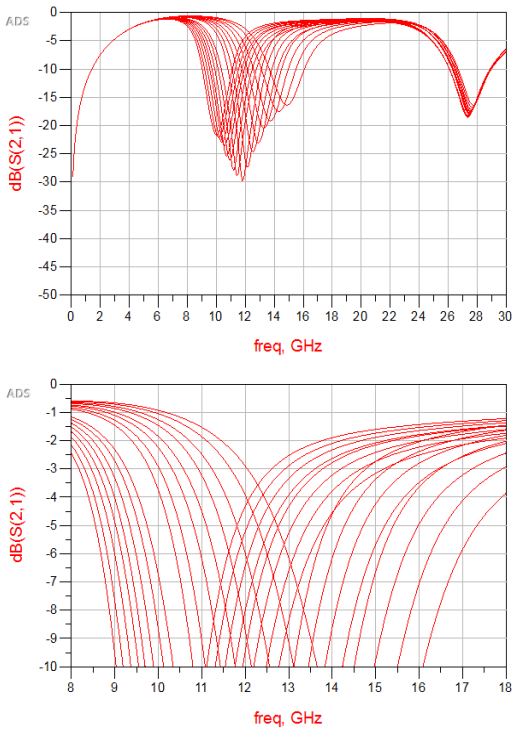

Figure 11:Composite band stop filter frequency response and match