High Performance GaN PA Design for 3.5 GHz 5G Applications

Careful designs utilizing Gallium Nitride technology for power amplifiers can ensure power, gain, and bandwidth requirements are met.

>> By By Robert Smith, David Collins, and Liam Devlin, Plextek RFI

Gallium Nitride-on-Silicon Carbide (GaN-on-SiC) is now a mature semiconductor technology used in an increasingly wide variety of RF applications. Power amplifiers (PAs) designed using commercially-available, packaged, discrete GaN transistors provide high-performance, cost-effective solutions to challenging technical requirements encountered in active phased-array radar and 5G systems.

The design of four different single-stage, high-efficiency power amplifiers for L-band radar applications using such transistors has been described by the authors in "The Design of High Performance L-band GaN PAs Using Commercially Available Discrete Transistors," in ARMMS Conference, U.K. The same GaN-on-SiC transistors have been used to design a two-stage power amplifier intended for 5G base stations operating in the 3.4–3.8 GHz frequency band. This covers the "Citizens Broadband Radio Service" band for shared wireless broadband use in the 3.55–3.7 GHz band (3.5 GHz band) that was defined by FCC in 2015, as well as the slightly wider band that has been designated for 5G use by Ofcom in the UK.

GAN PAS FOR RADAR APPLICATIONS

Table 1 summarizes the performance of two single-stage PAs for the 960–1215 MHz radar band, designed by Plextek RFI using commercially-available transistors fabricated on a high voltage Qorvo 0.25 μm GaN-on-SiC process. These PAs were designed to be operated in pulsed mode at 3 dB compression.

	QPD1010 PA	QPD1015 PA
Frequency Range	960–1215 MHz	960–1215 MHz
Output Power at 3 dB compression	40.4	47.7
PAE at 3 dB compression	65	60
Small-Signal Gain	19.5	19.7
Operating Voltage	50 V	50 V
Transistor Package	3 x 3 mm QFN SMD	Metal-ceramic air cavity flange

Table 1: Measured performance of L-band radar PAs.

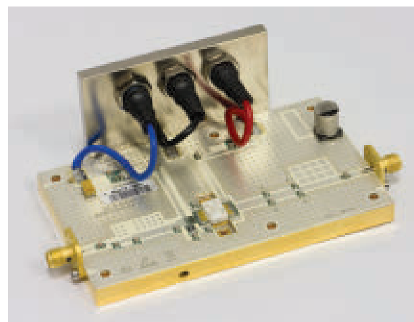

Figure 1: QPD1015 PA for L-band radar applications.

The QPD1010 transistor uses a low-cost 3 x 3 mm plastic Quad-Flat No Leads (QFN) surface-mount package, which allows for simpler PCB assembly. However, for higher power transistors such as the QPD1015, the superior thermal performance of metal-ceramic packages is required. High-power PAs require that significant attention be paid to thermal and power handling considerations. For the QPD1010 PA, copper-filled through-via holes are used to provide a low thermal impedance and low electrical inductance path to the metal carrier. For the QPD1015, the transistor is soldered directly to the aluminum carrier. A PCB metallization weight of 1 oz. copper, equivalent to a thickness of 35 μm, is necessary to handle the high DC current at the drain of the transistors when under high RF drive. The PCBs are bonded to custom aluminum carriers, which accommodate a metal side plate with banana jacks allowing convenient DC connections for testing.

A TWO-STAGE GAN PA FOR 3.5 GHZ 5G SYSTEMS

Unlike the PAs used for radar applications, those used in communications systems need to operate in continuous wave (CW) mode, backed off from saturation with high peak-to-average power ratio (PAPR) modulated signals. However, high output power is still required in many applications, and good power efficiency is essential to minimize electrical power

consumption. For the two-stage 5G PA described here, an output power of 50 W (47 dBm), small-signal gain of 25 dB, and input return loss of 10 dB were specified across a frequency range of 3.4–3.8 GHz. The PA was designed with 100 MHz of additional 'guard' bandwidth either side of the operating band to account for any design uncertainties and possible manufacturing and assembly tolerances.

DESIGN APPROACH

The QPD1015 transistor was selected for the output stage to provide the required level of output power. The driver stage transistor must produce enough power to drive the output stage without significant compression, which would degrade the cascaded IP3 performance. The QPD1010 transistor was selected for this purpose. Simulations undertaken using both the transistor simulation models and measured S-parameters indicated that the transistors would have sufficient gain at the design frequencies of interest. The fact that these transistors are specified to operate with a supply voltage of 50 V, instead of the standard 28 V, means that they draw less current for a given output power.

One of the first steps in the design process is to ensure in-band stability before designing the input and output matching networks. After stabilization, load-pull simulations are used to determine the output impedances to match to and the expected level of performance.

First designed and optimized separately, the two stages are then cascaded with the interstage matching network getting rationalized and optimized. Small tweaks to the input and output matching networks may be required to fine-tune the performance.

The matching networks are implemented as a mixture of lumped-element and distributed components, with SMT capacitors and resistors used in conjunction with microstrip transmission lines. Physically small capacitors were chosen to minimize parasitic effects from the packages. The resulting layout is then EM-simulated to account for coupling and fringing effects that are not included in the analytical models. Low-frequency decoupling networks are added to ensure stability, which can be problematic due to the high gain of GaN transistors at lower frequencies. The layout of the final EM-simulated metalwork is shown in Figure 2.

Frequency (GHz)	SS gain (dB)	Power (W)	PAE (%
3.3	25.68	52.9	44.78
3.4	25.74	64.2	50.4
3.6	25.68	64.1	51.9
3.8	26.34	59.2	55.1
3.9	25.95	52.6	57.2

Table 2: Simulated performance of a two-stage 5G GaN PA.

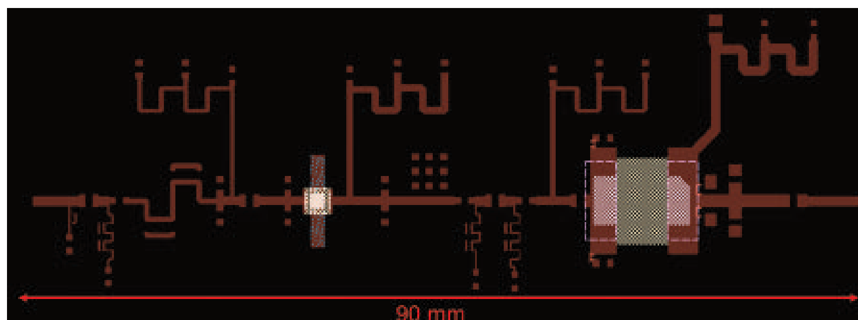

Figure 2: EM-simulated metalwork of a 3.4–3.8 GHz 50 W PA for 5G applications.

SIMULATED PERFORMANCE

Simulated S-parameters of the two-stage 5G PA are shown in Figure 3, and large-signal performance is outlined in Table 2.

FIGURES

It can be seen that the in-band gain flatness is very good, which is desirable for amplifying the wide-bandwidth signals that are likely to be used in 5G systems. Good input return loss makes the PA easier to integrate into a transmitter system while achieving high power from a single transistor minimizes the number of power combiners required in a transmitter, reducing both RF power losses and the size and weight of the transmitter. The in-band power added efficiency (PAE) is greater than 50 percent and the output power is over 50 W. WDD

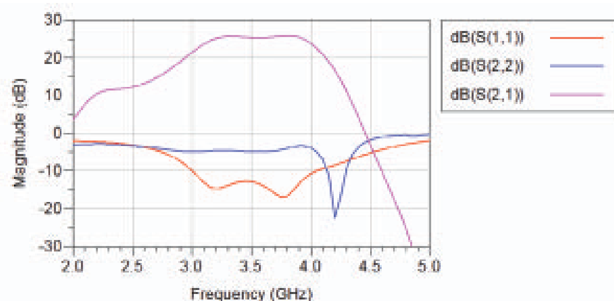

Figure 3: Small-signal performance of a two-stage 5G GaN PA.