# A Single Chip SMT Packaged 4-Channel mm-Wave 5G PA

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## Introduction

5G mobile devices operating at mmWave will incorporate electronic beam steering to address the difficulties of non-line of sight communications at these high frequencies. This requires the use of multiple parallel receive and transmit channels, which must be implemented in a low cost, compact manner. This presentation will describe the design of a 4-channel PA covering the 27.5 to 28.35GHz 5G band. It was realised as a single chip component on the 0.15µm E-mode GaAs PHEMT process of Sanan IC and is packaged in a standard over-moulded, 5mm x 5mm plastic QFN package. This results in a low cost, SMT compatible component suitable for incorporation into high volume commercial products. Each PA exhibits a gain of 20dB with an RF output power of 24.5dBm at 1dB gain compression with a PAE of 20%. When operated at 7dB back-off to preserve modulation fidelity the third order intercept point is 31dBm.

## 4-Channel mm-Wave 5G PA Architecture

Figure 1 depicts the block diagram of the 4-channel PA IC. It comprises of two halves which are exact mirror images of each other. Each half contains two identical channels, the top half contains channels 1 and 2 and the bottom half contains channels 3 and 4. Each channel is a 3 stage power amplifier with its own output power detector. The RF inputs and RF outputs of each channel are on the left and right hand sides respectively.

Channels 1 and 2 share the same DC bias pads/pins, which are depicted on the top side of the diagram. 'Vg12_CH12' is the gate bias voltage for stages 1 and 2 of channels 1 and 2, 'Vg3_CH12' is the gate bias voltage for stage 3 of channels 1 and 2. 'Vd12_CH12' is the drain supply for stages 1 and 2 of both channels and 'Vd3_CH12' is the drain supply for stage 3 of both channels. Sharing of the DC bias pads/pins allows for a compact form factor.

The nominal drain supply voltage is +4V and the gate bias voltages are adjusted to achieve the desired quiescent currents of 160mA in total for stages 1 and 2 (both channels of the commonly biased amplifier pair) and 240mA in total for stage 3, both channels. At this supply current each transistor is biased at a nominal current density of 100mA/mm.

The DC outputs of the RF power detectors for channels 1 and 2 are also located on the top side. 'Vdet_CH1' and 'Vdet_CH2' are the uncompensated detector outputs for channels 1 and 2 respectively and 'Vref_CH12' is the common detector reference voltage, shared between the channels. The temperature compensated detector output for channel 1 is given by 'Vref_CH12 - Vdet_CH1' and the equivalent for channel 2 is given by 'Vref_CH12 - Vdet_CH2'.

Due to mirror symmetry, the DC bias and power detector scheme described above equally applies to channels 3 and 4 where the DC pads are located on the bottom side of the diagram of Figure 1. As the part has been realised on an enhancement mode process, no negative voltages are required.

Biasing of the PA gates and monitoring of the power detector outputs can conveniently be done using widely available multi-channel DAC and ADC ICs.

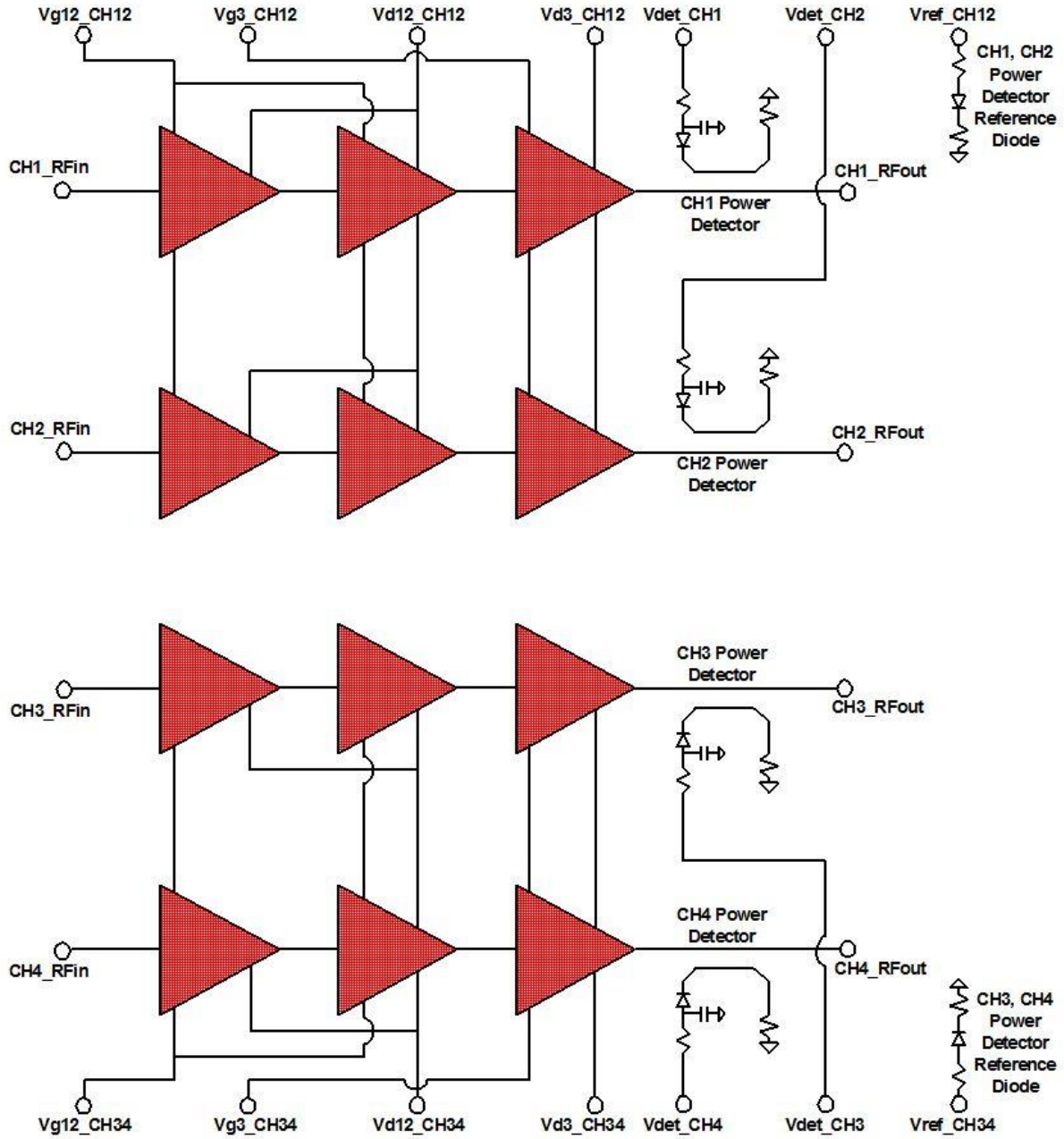


**Figure 1: Block Diagram of the 4-Channel PA IC**

Figure 2, below, shows a photograph of the 4-channel PA die. It measures just under 3.4mm x 3.4mm. Its pad / pin positions are similar to those shown in the block diagram of Figure 1 although it also incorporates a number of GND pads in order to make it fully RF on Wafer (RFOW) testable.

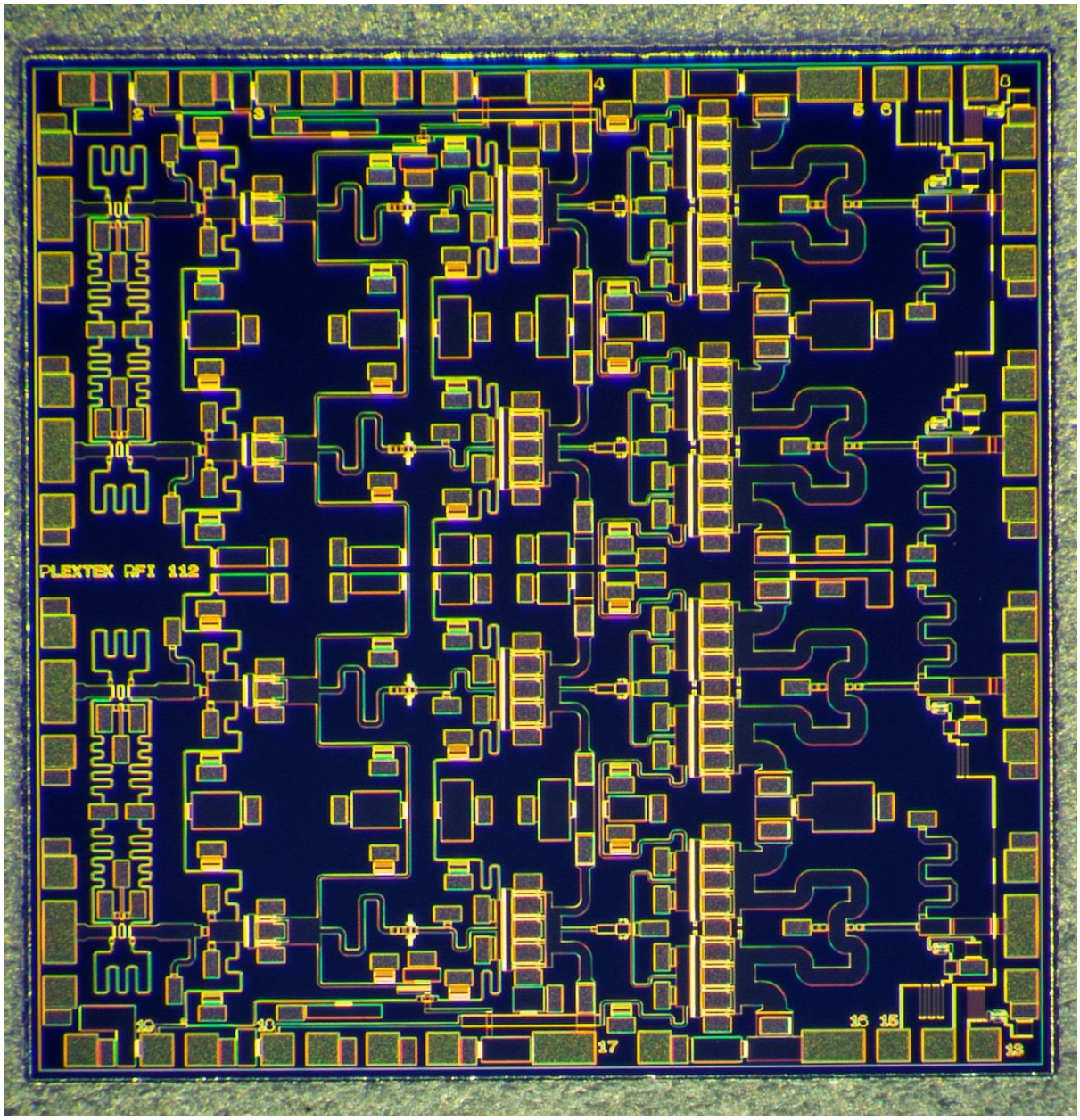


**Figure 2: Photograph of the 4-Channel PA die**

## Single Channel Measured Performance

An evaluation PCB was designed using a low cost laminate PCB material suitable for volume mass production. Samples of SMT packaged 4-channel PAs were assembled on to the evaluation PCBs; all of the measured performance is calibrated to the package pins and includes the effects of the IC to PCB transition. A TRL calibration tile was designed to allow the calibration of the measured performance to the reference planes of the package. A photograph of one of the 4-channel PAs mounted on an evaluation PCB is shown in Figure 3.

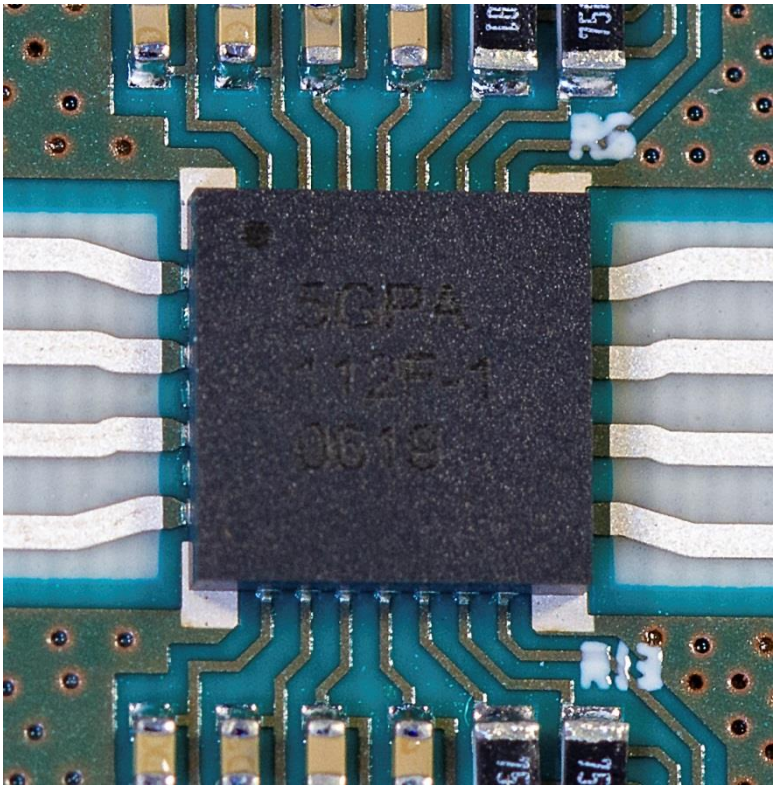


**Figure 3: Photograph of the SMT Packaged 4-Channel PA on EVB**

All measurements presented below were carried out on a single channel (channel 2) of a typical device at room temperature biased at a quiescent current density of 100mA/mm from +4V.

Figure 4 shows the measured s-parameters of the packaged PA (channel 2) on its evaluation PCB. The gain is around 19.6dB ±1.4dB across 26GHz to 29GHz and the input and output return losses are around 10dB across the band.

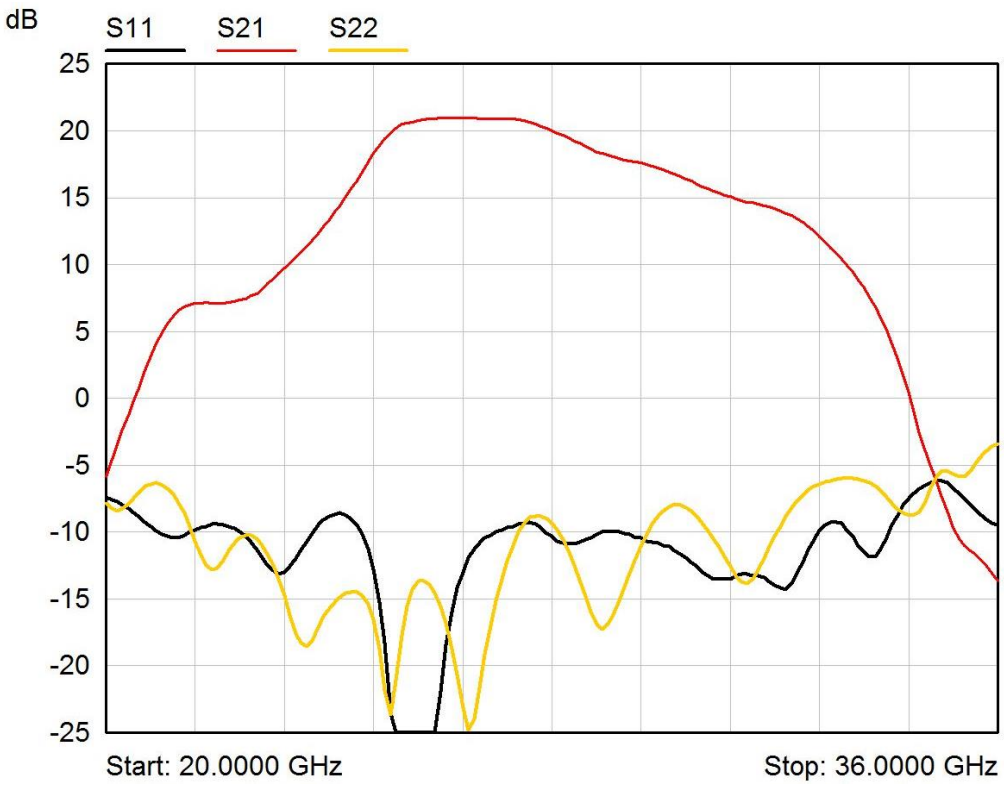


**Figure 4: Measured S-Parameters**

Figure 5 compares the measured gain response with simulation, the red trace is measured and the blue trace is simulated. The simulated performance includes EM simulation of all matching networks.

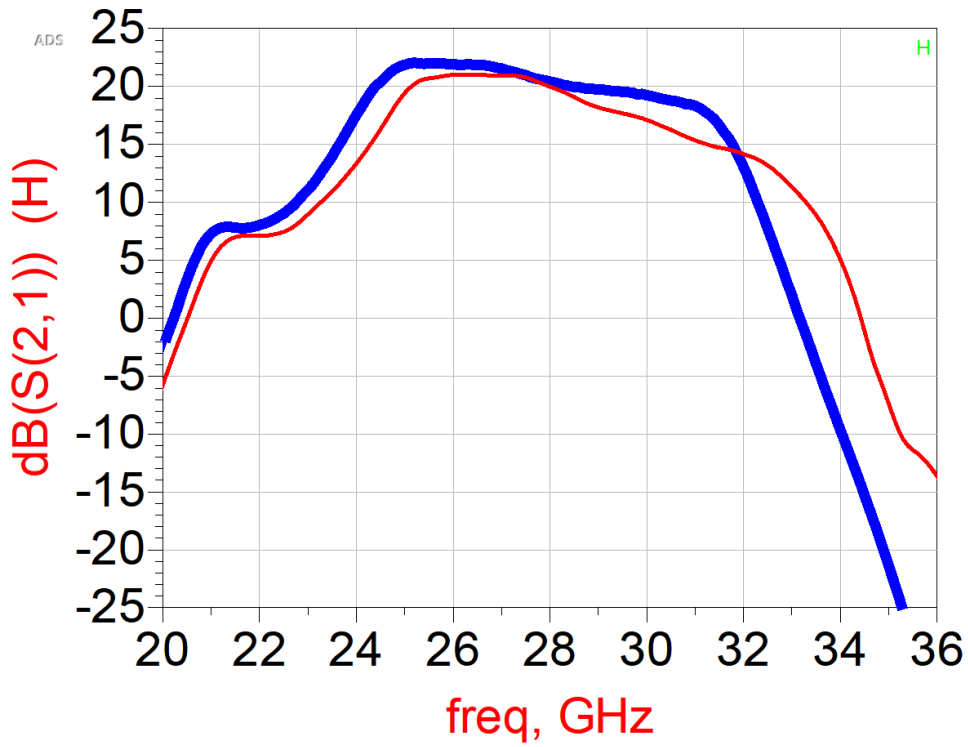


**Figure 5: Measured Gain (red) Vs Simulated Gain (blue) at 100mA/mm bias**

Although the PAs for 5G systems will operate backed-off to provide linear amplification and preserve modulation fidelity, the RF output Power at 1dB gain compression (P-1dB) was measured to provide a figure of merit for comparative purposes. This is plotted versus frequency in Figure 6 along with the associated Power Added Efficiency (PAE). The typical P-1dB is around 24.5dBm with a corresponding PAE of around 19.5%. Figure 7 shows a similar plot for the measured RF output power at saturation (Psat) and corresponding PAE which are typically around 25.5dBm and 21.5% respectively.

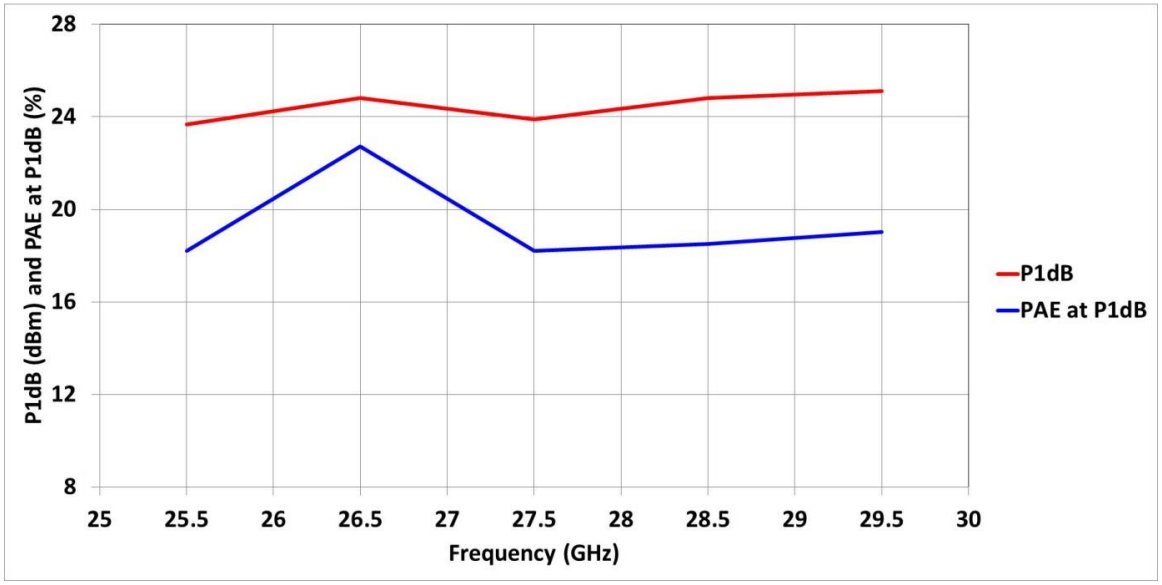


**Figure 6: Measured P1dB and PAE at P1dB Vs Frequency**

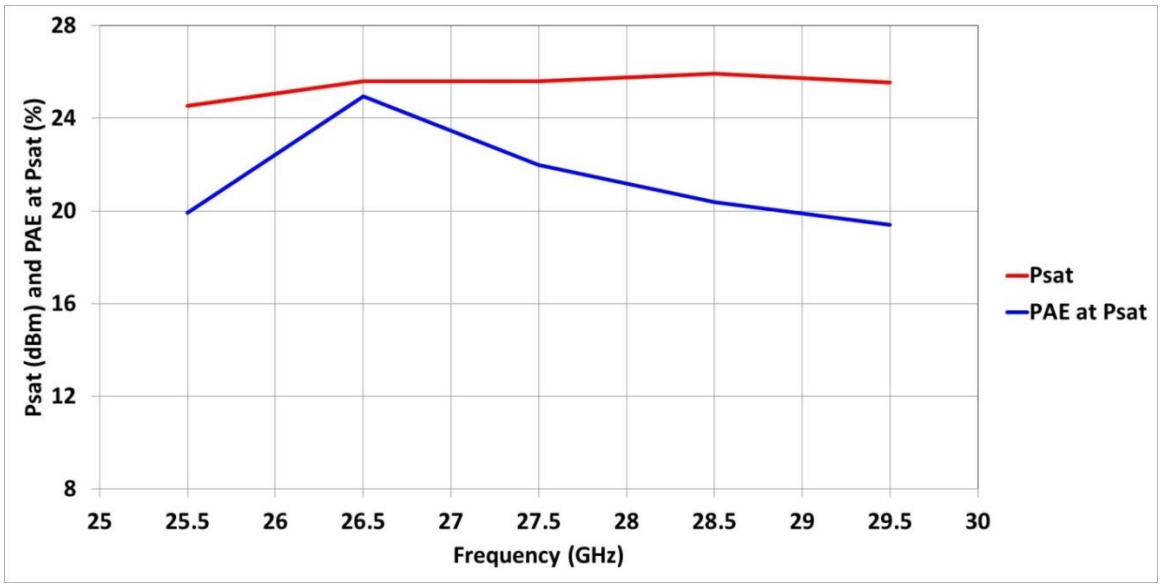


**Figure 7: Measured Psat and PAE at Psat Vs Frequency**

To reflect the wide channel bandwidths anticipated in 5G systems, the output referred third order intercept point (OIP3) was evaluated with a tone spacing of 100MHz. The measured OIP3 is plotted in Figure 8 at an output power of around +8dBm per tone. It can be seen that the OIP3 is on average

around +31dBm across the 26GHz to 29GHz band. Measured IMD3 vs total output power was also plotted and is shown in Figure 9. The different trace colours in the IMD3 plot represent different measurement frequencies and the IMD3 (in dBc) is plotted against the total RF output power. This indicates that at an operating point of +17.5dBm, corresponding to around 7dB back-off, the corresponding IMD3 is around -30dBc or better across the band.

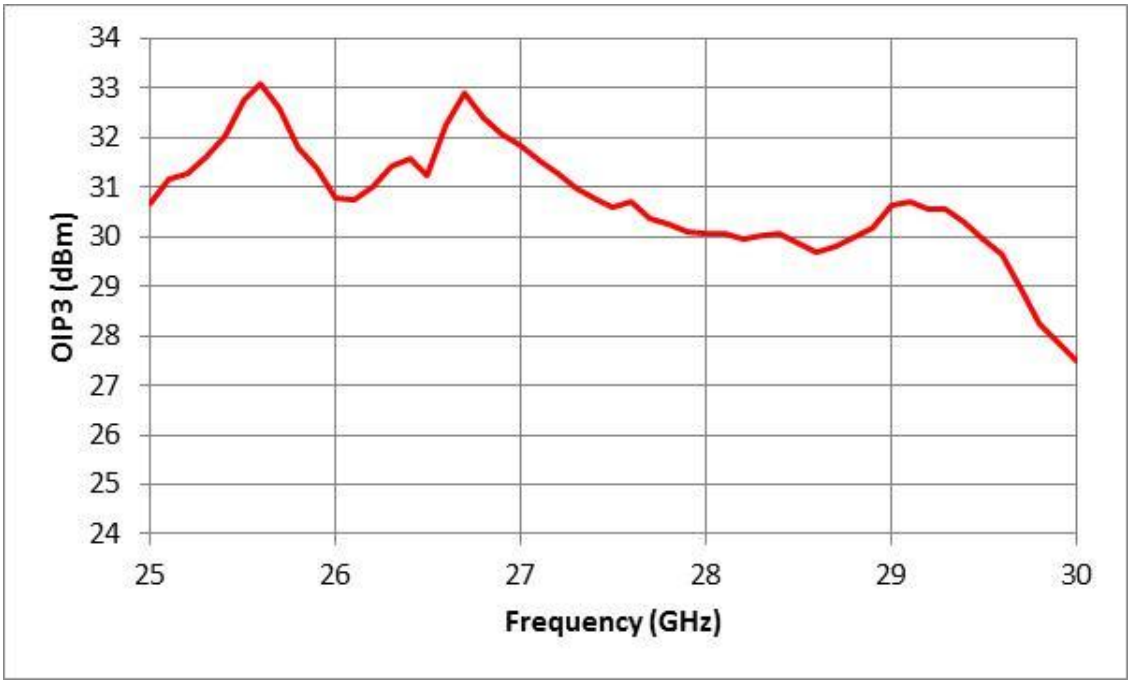


**Figure 8: Measured PA OIP3**

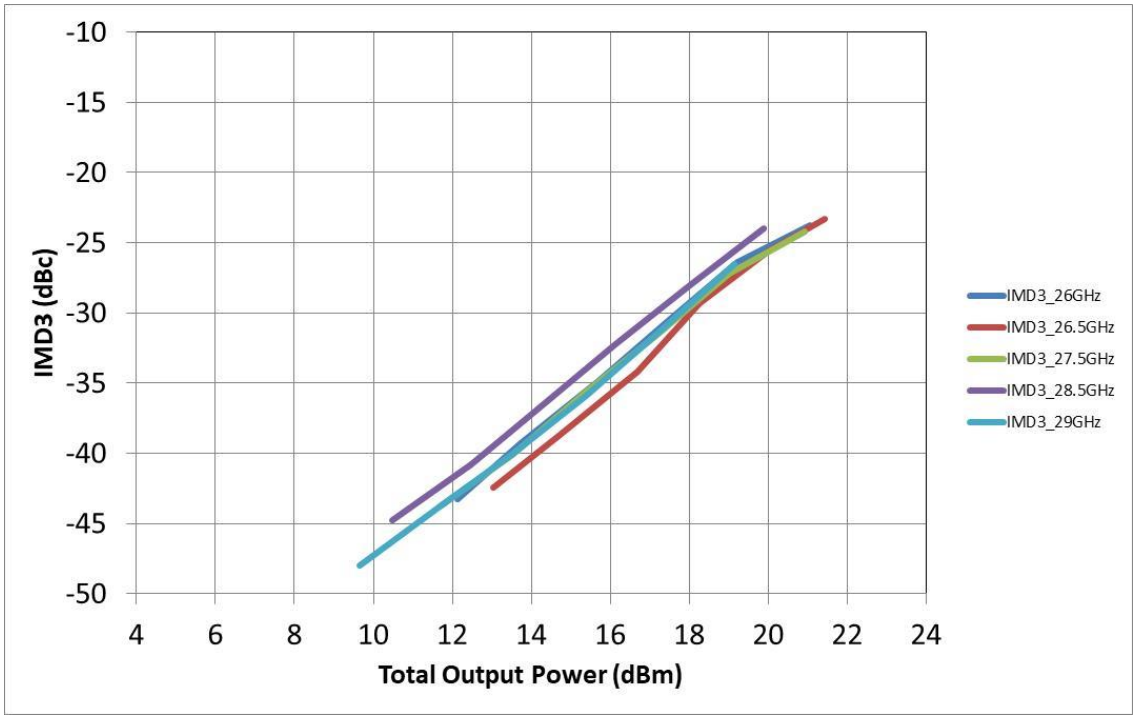


**Figure 9: Measured IMD3 Vs Total Output Power Vs Frequency**

Drive up curves showing PAE against total RF output power were measured and are plotted below in Figure 10. As with the IMD3 measurements the different trace colours represent different measurement frequencies. This indicates that at a +17.5dBm operating point (around 7dB back-off), the PAE is at least 6% across the band.

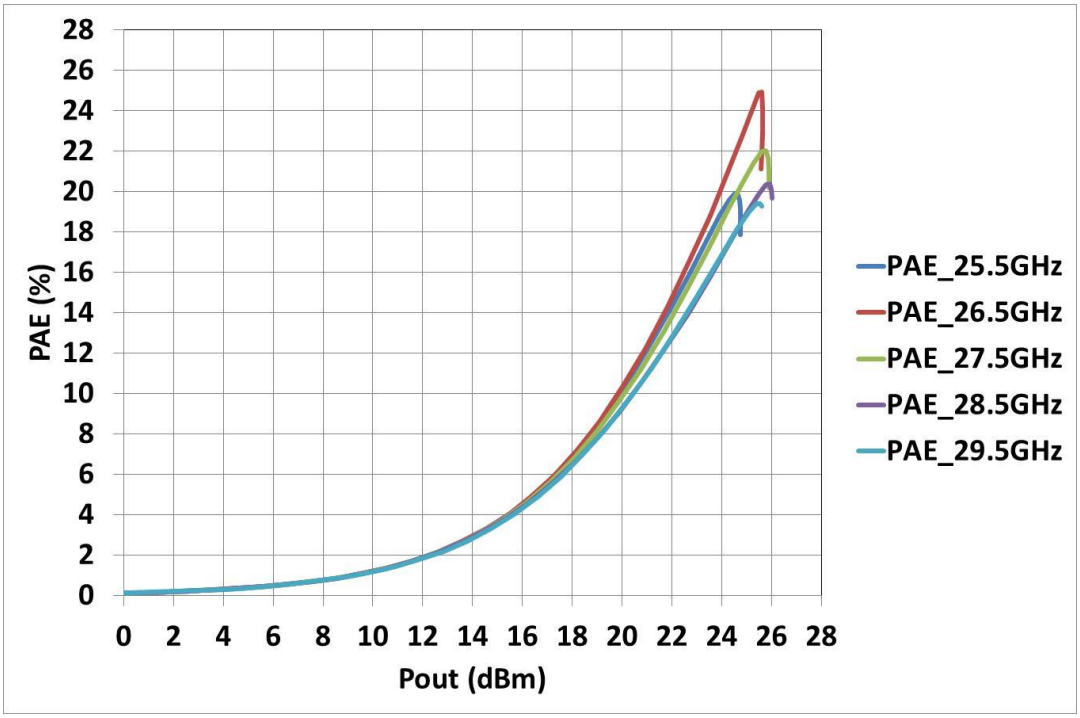


**Figure 10: Measured PAE Vs Output Power Vs Frequency**

The on-chip Tx power detector generates a DC voltage that allows monitoring of the RF output power. Figure 11 is a plot of the temperature compensated detector output 'Vref_CH12-Vdet_CH2' in mV on a logarithmic scale against RF output power in dBm at 27.5GHz over an 18dB dynamic range. It can be seen that the characteristic is linear which simplifies power monitoring and control.

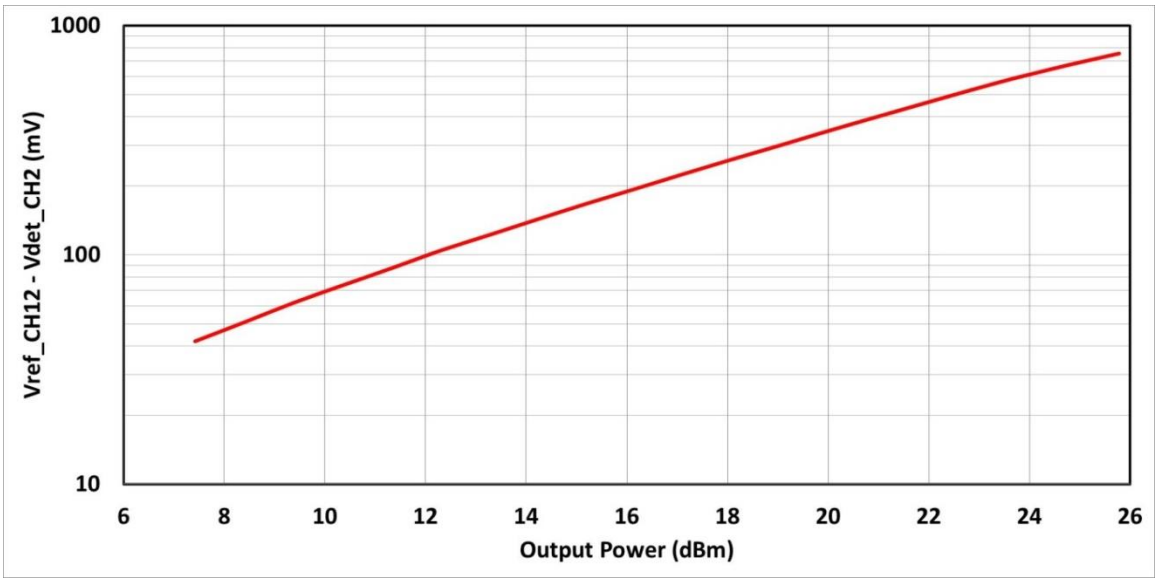


**Figure 11: PA On-Chip Power Detector Measured Characteristic at 27.5GHz**

A summary of the measured performance of one of the 4 channels of the SMT packaged PA is provided in Table 1, below.

| Parameter | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|
| Frequency Range | 26 | | 29 | GHz |
| Gain | | 19.6 | | dB |
| Input Return Loss | | 10 | | dB |
| Output Return Loss | | 10 | | dB |
| P1dB | | 24.5 | | dBm |
| Psat | | 25.5 | | dBm |
| PAE at P1dB | | 19.5 | | % |
| PAE at Psat | | 21.5 | | % |
| OIP3 | | 31 | | dBm |
| RF power at 7dB back-off | | 17.5 | | dBm |
| IMD3 at 7dB back-off | | -31 | | dBc |
| PAE at 7dB back-off | | 6.0 | | % |

**Table 1: Measured Performance Summary of a Single Channel**

## Four Channel Performance

If the 4 PAs are driven with coherent RF signals and are used to drive a suitable 4-element antenna array the RF output signals will combine to provide a 6dB increase in RF power ($10.Log_{10}(N)$, where N is the number of elements). By appropriately setting the phases of the signals to the 4 antenna elements it is possible to electronically steer the direction of the antenna beam. The summary performance shown in Table 2 assumes identical PA performance and excludes output routing losses and provides an indication of the effective performance that could be achieved from a 4 element array. The gain of each antenna element will also add to the total Effective Radiated Isotropic Power (EIRP) to further increase these parameters.

| Parameter | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|
| Frequency Range | 26 | | 29 | GHz |
| Number of Elements | | 4 | | _ |
| Effective P1dB | | 30.5 | | dBm |
| Effective Psat | | 31.5 | | dBm |
| Effective OIP3 | | 37 | | dBm |
| Effective RF power at 7dB back-off | | 23.5 | | dBm |

**Table 2: Four Channel Performance Summary**

## Application of the 4-Channel mm-Wave 5G PA

A block diagram showing the 4 channel PA in a 5G transmitter (Tx) beamforming application is shown below in Figure 12.

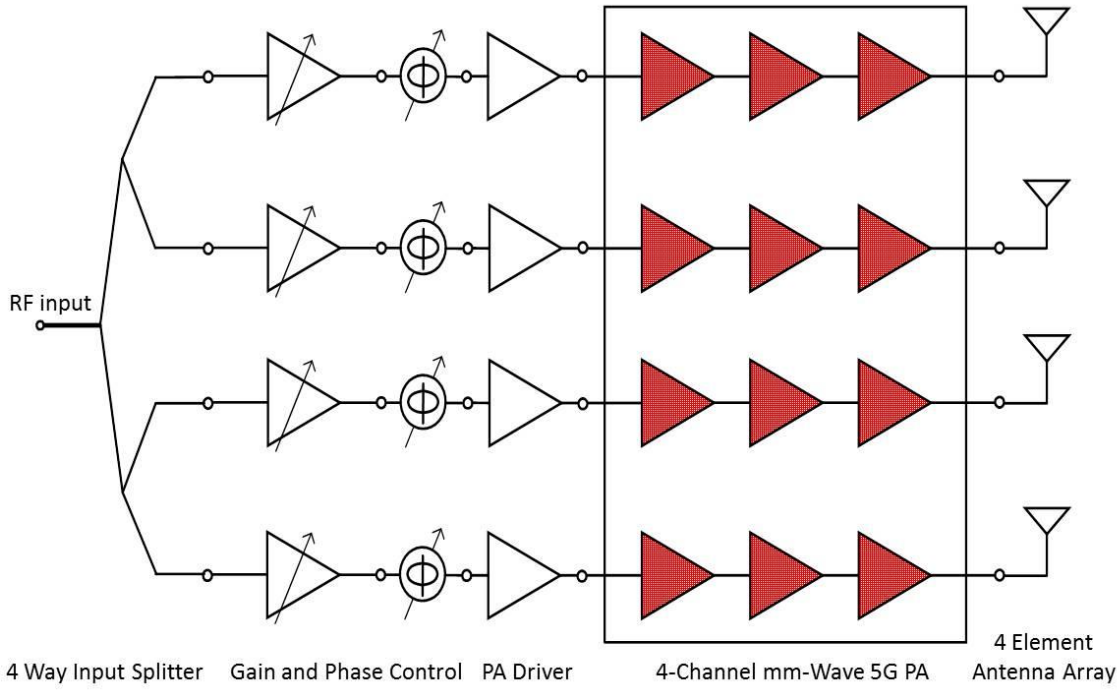


**Figure 12: Application of the 4-Channel mm-Wave 5G PA**

The application depicted in Figure 12 uses an analogue beamforming architecture with four antenna elements. The mm-wave RF input is split into four and feeds each of four channels. Within each channel there is independent gain and phase control for beam optimisation followed by a PA driver. Up to this point all functions can be integrated on a Silicon RFIC (Radio Frequency Integrated Circuit). Several vendors are now offering such solutions, typically implemented in SiGe (Silicon Germanium) but CMOS products are also in development. On their own, these solutions seem sufficient for addressing lower EIRP 5G terminal applications such as user terminals and local area base-stations. When used in conjunction with the 4 channel PA, implemented in GaAs PHEMT, higher EIRP applications such as medium range and wide area base-stations can also be addressed.

The 4 element antenna array can be implemented as either an array of 1 x 4 or 2 x 2 patch antennas printed on an appropriate low loss laminate material. The compact SMT package in which the 4 channel PA is housed allows it to be conveniently mounted in close proximity to these antennas so as to minimise losses.

Figure 12 depicts the four antenna elements dedicated to Tx only, this is a possibility meaning that a corresponding receiver (Rx) will also need a dedicated antenna array. Another possibility is that each antenna element can be shared between a Tx and an Rx channel. Typically in time division duplex (TDD) systems such as 5G NR this is done by means of a single pole dual throw (SPDT) switch which alternately routes Tx and Rx to the antenna and provides isolation between the two channels. An

alternative approach is to have the Tx and Rx channels permanently routed to orthogonal ports of the same antenna element, isolation between the channels is then achieved due to Tx and Rx having orthogonal polarisations. A benefit of the 4 channel PA being realised on an enhancement mode process is that during Rx modes it can conveniently be powered down by pulling the gates to 0V.

Although the application described above uses a 4 element antenna array, use of the 4 channel PA can easily be extended to larger arrays. For example, if the number of elements in the array were 16, then this would require the use of four of the 4 channel PAs in parallel.

## Summary and Conclusions

The 4-channel PA MMIC described here offers a compelling solution for 5G terminals which necessitate the deployment of multiple power amplifiers. The part demonstrates good performance from 26GHz to 29GHz so is suitable for the full 28GHz 5G band. A temperature compensated output power detector is included on all channels.

Realised on a state of the art 0.15µm enhancement mode GaAs P-HEMT process, the part is easy to bias and monitor using widely available multi-channel DAC and ADC ICs. In addition, the part is conveniently housed in an extremely compact and low cost 5mm x 5mm plastic overmoulded QFN SMT package and is suitable for high volume, low-cost production.

The 4 channel PA can be used to address 5G terminal applications requiring higher EIRP such as medium range and wide area base stations which cannot be addressed by Si RFIC solutions alone.