Case Study – Single Chip Front End Module (FEM) for 28GHz 5G

With the roll-out of 5G expected in the very near future, the research activities of the industry's key players are now well under way and have reached the point where custom mm-wave components are being specified, designed and evaluated. An essential component required to enable future mm-wave 5G systems is the Front End Module (FEM) providing the final stages of amplification in a transmitter and the earliest stages of amplification in a receiver in time division duplex (TDD) systems. The FEM must demonstrate high linearity in transmit mode (Tx) and low Noise Figure in receive mode (Rx). Furthermore, as mm-wave 5G systems are likely to require multiple FEMs to be deployed in each terminal as part of a phased array or switched antenna beam architecture, they must also be highly efficient, compact and low cost. Ease of control and monitoring is also highly desirable in such applications.
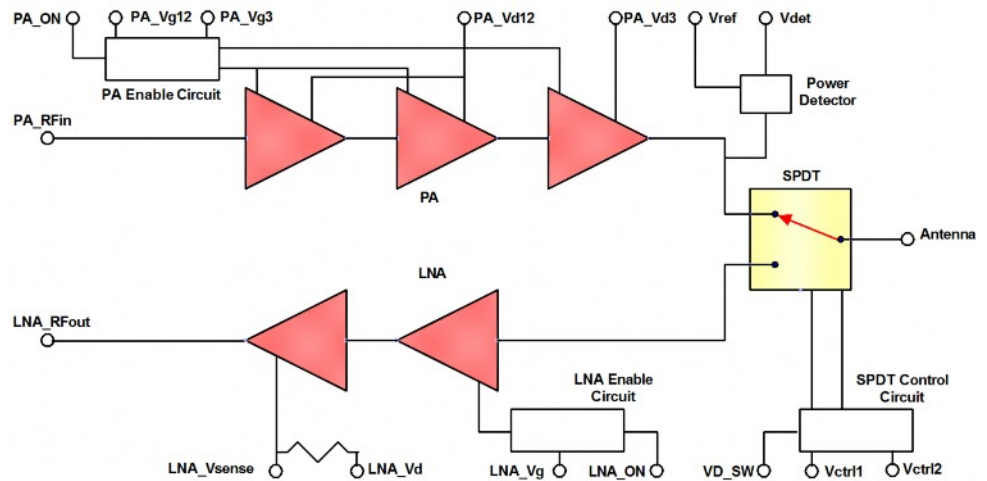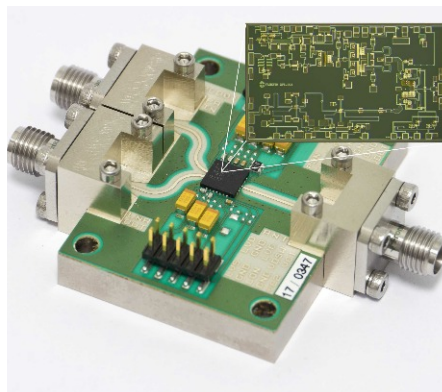
Figure 1: Block Diagram of FEM MMIC for 28GHz 5G

This case study describes the design and evaluation of an SMT packaged FEM MMIC for the 28GHz 5G band (27.5 to 28.35GHz) which satisfies all of the requirements outlined. The part was developed by PRFI and fabricated on WIN Semiconductor's PE-15 process which is a 4V, 0.15µm, enhancement mode GaAs P-HEMT process. It is conveniently housed in a compact and low-cost 5mm x 5mm plastic overmoulded SMT compatible QFN package. The part can be readily controlled and monitored by widely available multi-channel ADC and DAC circuits. It easily covers 27GHz to 29GHz and so encompasses the full 28GHz 5G band.

A block diagram of the FEM MMIC is shown above. The transmit signal path runs from left to right in the top half of the diagram; the input is at the pin labelled 'PA_RFin'. The signal is amplified by a 3 stage PA and then routed to the Antenna via a single pole double throw (SPDT) switch. A temperature compensated power detector is included to allow monitoring of the transmitted RF output power. The compensated detector output is given by the difference between the voltages 'Vref' and 'Vdet'. A fast switching enable circuit 'PA Enable Circuit' is also featured and is controlled by the (active low) logic signal 'PA_ON'. This is used to rapidly power up and power down the PA when switching between Tx and Rx modes such that it draws a mere 0.1mA when not in use, maximizing overall system efficiency. In the enabled state the PA is biased in deep class AB for good efficiency at back-off, positive gate bias voltages are applied at pins 'PA_Vg12' and 'PA_Vg3' of around +0.45V. The PA runs from a +4V drain supply applied at 'PA_Vd12' and 'PA_Vd3'.

The SPDT switch can be controlled by a single bit, 'Vctrl1', which is set to +4V for Tx mode or 0V for Rx mode. Single bit control is facilitated by the 'SPDT Control Circuit' which is essentially a 1 to 2 line decoder. The combined supply current drawn by both the control circuit and the SPDT itself is just 1mA from the +4V applied at 'VD_SW'.
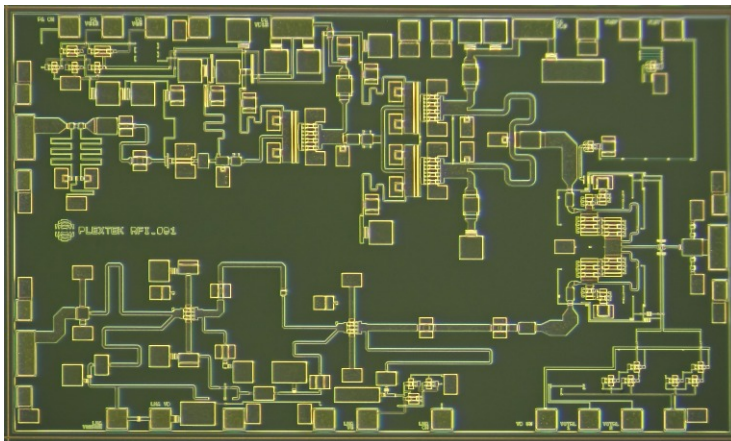
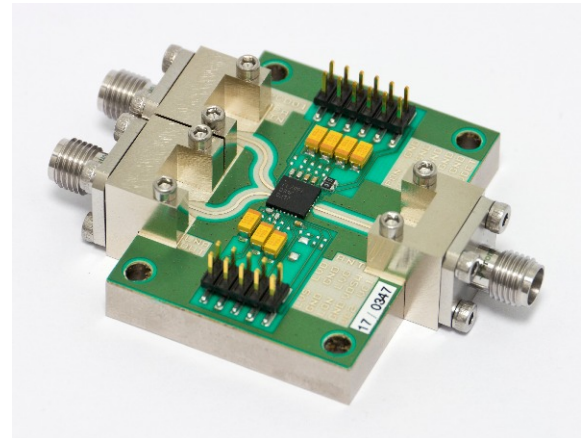**Figure 2: Die Photograph of FEM MMIC**

Figure 3: Photograph of Packaged FEM on a Laminate Evaluation PCB

The input to the receive path is at the 'Antenna' pin, which is routed to the input of a 2 stage LNA by the SPDT. The output of the receive path is at the pin labelled 'LNA_RFout'. As with the PA, the LNA also has a fast switching enable circuit such that the LNA draws as little as 0.1mA when not in use. When enabled, the LNA requires just 10mA of DC supply current from its +4V supply. The gate bias voltage (of around +0.55V) is applied at pin 'LNA_Vg' and the 4V drain bias is applied at 'LNA_Vd'. The 'LNA_Vsense' pin is provided to allow for bias current monitoring. When correctly biased this pin is at 3.9V.

A photograph of the FEM die is shown above.

The FEM MMIC die measures just 3.38mm x 1.99mm. Its pad / pin positions are similar to those shown in the block diagram, although it incorporates a number of GND pads in order to make it fully RF on Wafer (RFOW) testable. It was designed to be packaged in a low-cost plastic overmoulded 5mm x 5mm QFN and the effects of the overmould and the package transi-

tion were key considerations during the design process. Die were tested RFOW, which confirmed that the first pass design had been successful prior to packaging.

A photograph of one of the packaged FEMs mounted on a low-cost laminate evaluation PCB is shown above. A TRL calibration standard was also fabricated to allow measured performance parameters to be easily referenced to the package's RF pins.

Evaluation results for the packaged FEM MMIC mounted on the PCB and referenced to the package's RF pins are shown overpage. Throughout the evaluation, a multi-channel DAC and ADC IC was used to control and monitor the FEM. Conveniently, the FEM does not require any negative voltages as it was designed on an enhancement mode process.

Measured s-parameters of the Tx path of a typical FEM on the evaluation PCB are shown in Figure 4. In this mode the LNA is powered down, the SPDT control bit 'Vctrl1' is toggled high and the PA biased to around 70mA total quiescent current from

+4V. Small signal gain (S21) is 17.1dB ±0.4dB from 27GHz to 29GHz. The input return loss (S11) is better than 18dB across the band. The output is matched for best PAE at back-off and has an output return loss (S22) of 8dB or better across the band.

The measured output referred third order intercept point (OIP3) of the Tx path versus frequency is plotted at different wanted output tone powers ranging from 1dBm per tone to 11dBm per tone in Figure 5. The tones were spaced 100MHz apart. The OIP3 is around +28dBm across the 5G band and shows very little variation with tone power over a 10dB dynamic range.

Figure 6 shows the measured output power of the Tx path at the antenna pin against frequency. The RF output power is around 21dBm at saturation and around 20.2dBm at 1dB compression. The trace labelled 'Power at IMD3=35dBc' refers to the total output power at which the third order intermodulation products (IMD3) are 35dB below the wanted products during a 2-tone test with 100MHz tone spacing. At this point the part is operating at around 7dB backed-off from P1dB and
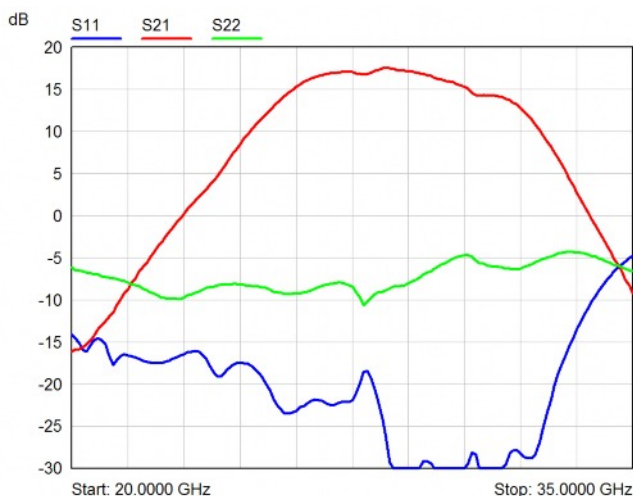
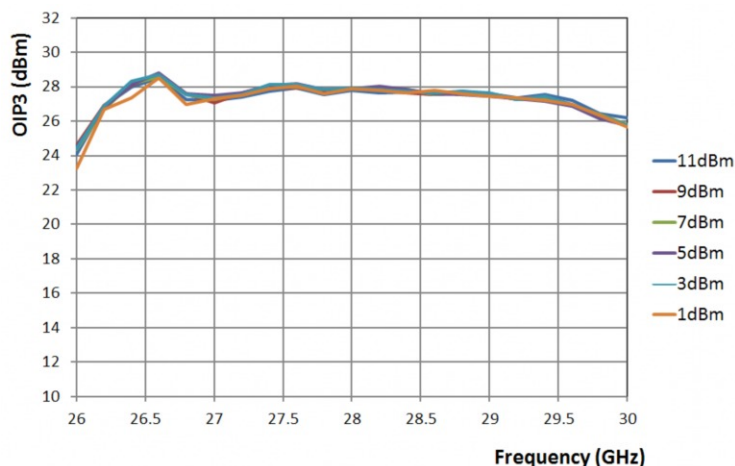**Figure 4: FEM TX Path Small Signal S-Parameters**

Figure 5: FEM Tx OIP3 Vs Frequency Vs Output Tone Power (100MHz tone spacing)

is closer to what would be the normal average operating power in a 5G system. An important goal of the design process was to maximize the efficiency at this operating point.

The measured power added efficiencies (PAE), at the antenna pin, at P1dB and at back-off are shown against frequency in Figure 7.

PAE at 28GHz and 1dB compression is slightly greater than 20%. When backed-off to the point at which IMD3 reaches 35dBc the part achieves a PAE of 6.5%. This is an excellent result and is largely due to the PA being designed to operate in deep class AB.

The on-chip Tx power detector produces a temperature compensated output voltage 'Vref-Vdet'. The detector's voltage is linear with RF output power (in dBm) for output powers from 6dBm to 21dBm (the Psat of the PA).

The Rx path performance is shown next. In this mode the PA is powered down, 'Vctrl1' is set to 0V and the LNA biased to around 10mA from +4V with 3.9V observed on the 'LNA_Vsense' pin.

The measured small signal gain and Noise Figure are plotted against frequency in Figure 8. Gain is around 13.5dB with a flatness of just ±0.3dB across the band.
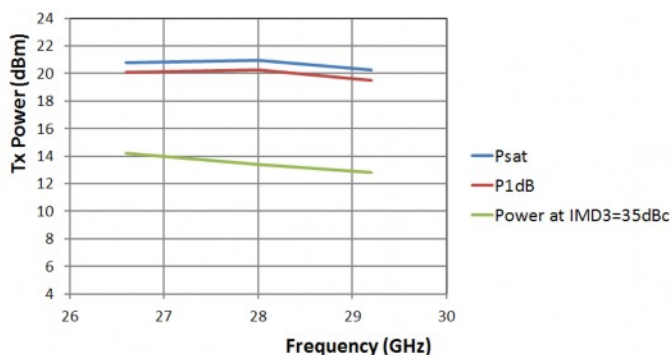

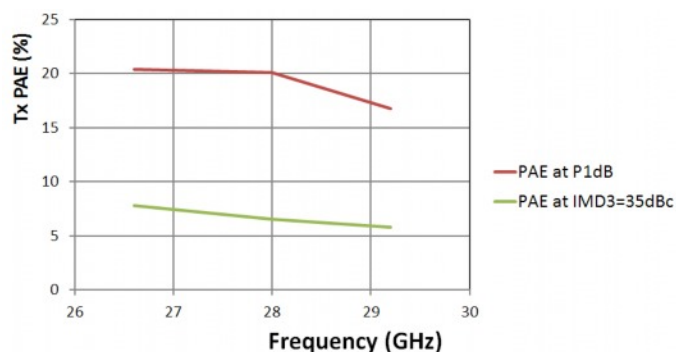**Figure 6: FEM Tx Path Output Power Vs Frequency**

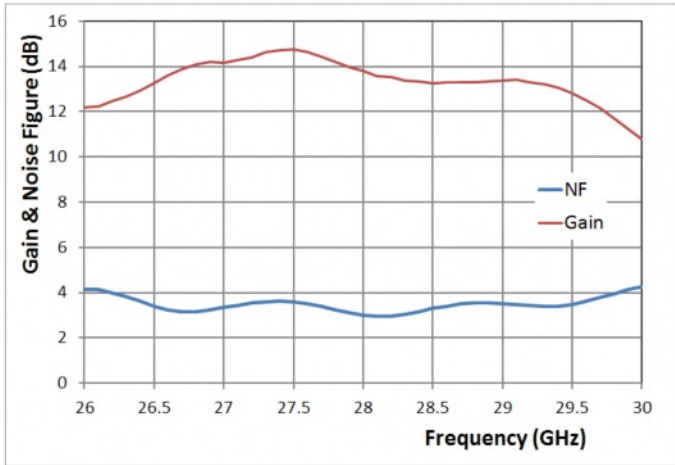**Figure 7: FEM Tx Path PAE Vs Frequency at P1dB and at Back-Off**

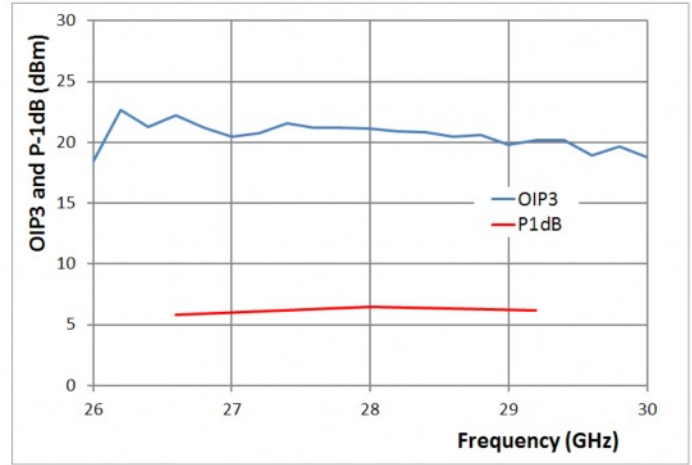**Figure 8: FEM Rx Noise Figure & Small signal Gain**

Figure 9: FEM Rx P1dB & OIP3

The Rx path has an excellent Noise Figure of typically 3.3dB from 27GHz to 29GHz band.

The Rx path also demonstrates impressive linearity for the modest power consumption. Key parameters such as P1dB and OIP3 are around 6.2dBm and 21dBm respectively across the band and are plotted in Figure 9.

The FEM MMIC described in this case study will potentially play a vital role in future 28GHz, 5G systems. The part has been shown to address all the requirements for integration into mm-wave phased-array terminals and offers excellent Tx linearity and efficiency together with outstanding Rx Noise Figure. The part also features a Tx power detector, Tx and Rx enable circuits, an SPDT decoder circuit and Rx bias monitoring. Realised on a state of the art 0.15μm enhancement mode GaAs PHEMT process, the part is extremely easy to control and monitor using widely available multi-channel ADC and DAC circuits. In addition, the part is conveniently housed in a compact and low cost 5mm x 5mm plastic overmolded QFN SMT package, making it well suited to high volume usage.