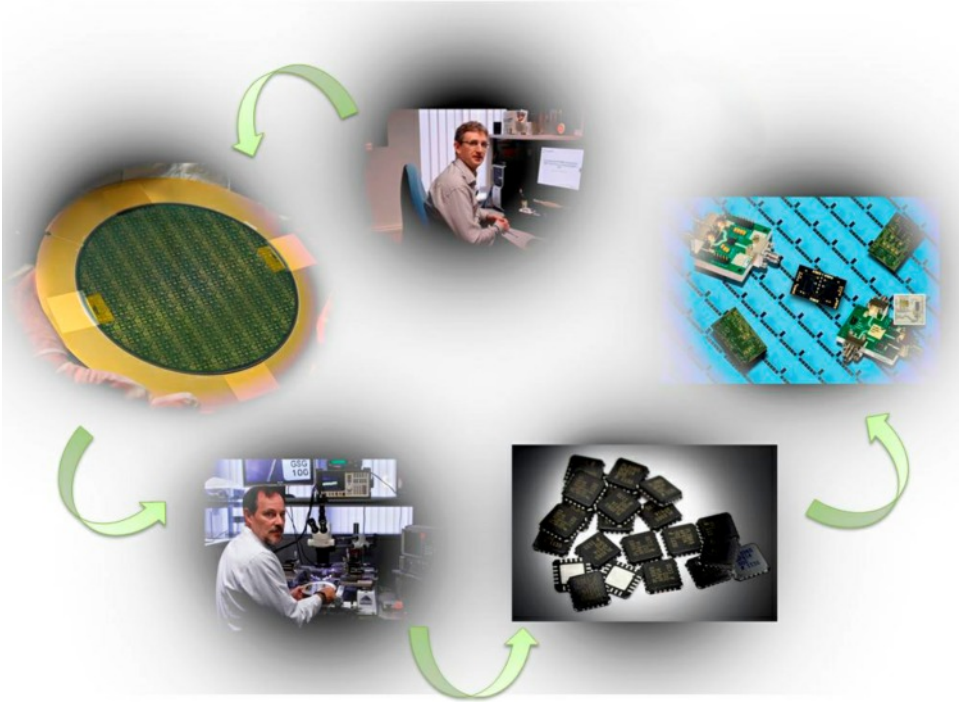
PRFI Closes the Gap between Measured and Modelled MMIC Performance



Custom designed MMICs allow the desired functionality and performance to be optimised whilst minimising size and potentially reducing production costs. Whilst the upsides are clearly attractive, the consequences of a custom designed MMIC failing to meet the required performance criteria can be costly. As well as the expense of the re-design and a second fabrication run, the detrimental impact on project timescales can be even more costly. First time right design success is therefore highly sought after and it is the ability to consistently and accurately predict performance prior to manufacture that allows this.

Introduction

This white paper reviews some recent MMIC designs carried out by PRFI that demonstrate how highly accurate MMIC performance predictions can be achived. Close agreement between measured and modelled performance is exhibited across a wide range of circuit functions, operational frequencies and process nodes and all designs were first pass successes. Insight is also given into the design methodology associated with the development of these MMICs, in particular detailed EM simulation is essential to achieve such close agreement. All of the designs presented were developed using ADS from Keysight.

The following design examples are presented:

- 3rd Order Elliptical High Pass Filter for the 39GHz 5G Band
- 6 to 18GHz Single Stage Feedback Amplifier
- Power Amplifier MMIC for the 26GHz 5G Pioneer Band
- 6 to 23GHz Double Balanced Mixer
- 20 to 30GHz SPDT Switch MMIC for 24GHz, 26GHz and 28GHz 5G bands
- SMT packaged mm-wave MMICs

PRFI Ltd.
The Plextek Building, London Road, Great Chesterford,
Saffron Walden, CB10 1NY, UK

T: +44 (0) 1799 796464 **E:** enquiries@prfi.com **W:** www.prfi.com

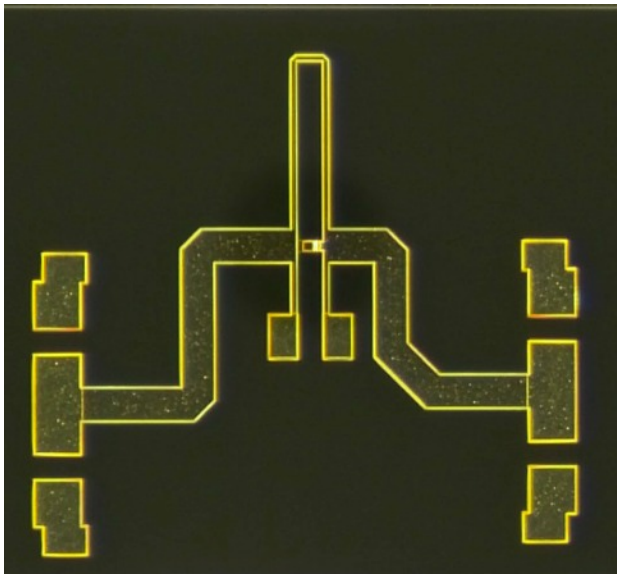


Figure 1: Photograph of 3rd order elliptical high pass filter test cell

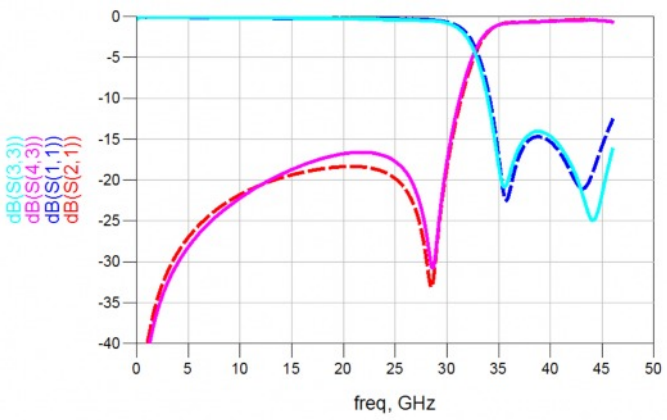


Figure 2: Comparison of measured to simulated

3rd Order Elliptical High Pass Filter for the 39GHz 5G Band

This filter was designed as part of a multi-function 5G MMIC addressing the 37GHz (37 – 38.6GHz) and 39GHz (38.6 – 40GHz) 5G bands. Its purpose was to provide rejection below band with low insertion loss across the full RF operating band. It was fabricated on one of WIN Semiconductors' 0.15µm InGaAs pHEMT processes. The filter was realised as an independently testable sub-circuit, as shown in the photograph of Figure 1.

The design process commences with the realisation of a simple elliptic filter using ideal capacitors and inductors (Ls and Cs). The capacitors are then replaced by Metal Insulator Metal (MIM) capacitors from the foundry PDK (Process Design Kit) and the filter is re-optimised. This stage is normally straightforward and has minimal impact on performance. The inductors are then replaced with high impedance transmission lines, again using the foundry PDK models. The filter is again re-optimised. Layout of the filter is now undertaken with every effort being made to minimize layout parasitics.

The next stage of the design process is the most critical and time consuming and must be completed with great care in order to obtain good measured to modelled performance. The layout must be EM simulated, step by step with careful optimisation of the design and layout at each step to maintain optimum performance. Determination of the most appropriate mesh density is a compromise between simulation speed and accuracy. In the case of this filter, the input and output 50Ω routing track were also included in this process. They link to adjacent blocks in the multi-function MMIC and have a significant impact on the performance of the filter.

Figure 2 compares the RFOW measured performance of the filter sub-circuit to the simulated. The solid traces are the measured response and the dashed traces the simulated. Excellent agreement between measured and modelled is demonstrated to beyond 40GHz.

6 to 18GHz Single Stage Feedback Amplifier

The single stage feedback amplifier shown in Figure 3 is, like the filter, a sub-circuit from a larger multi-function MMIC. This is a wideband 6 to 18GHz gain block designed on a WIN Semiconductor 0.25µm GaAs PHEMT process. It uses shunt resistive feedback to cover the full 6 to 18GHz band with a flat gain versus frequency response and good input and output return losses.

The measured versus modelled s-parameters are plotted in Figure 4 below. Measured results were made RFOW and are shown in blue with simulated performance in red. Agreement between measured and modelled performance is again excellent.

PRFI Ltd.
The Plextek Building, London Road, Great Chesterford,
Saffron Walden, CB10 1NY, UK

T: +44 (0) 1799 796464 **E:** enquiries@prfi.com **W:** www.prfi.com

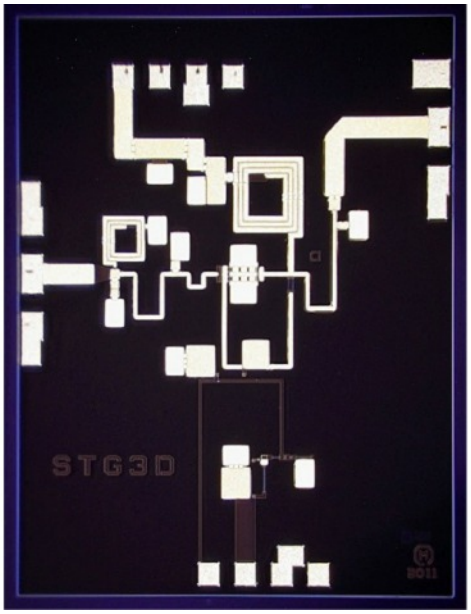


Figure 3: Die photograph of the 6 to 18GHz single stage amplifier test cell

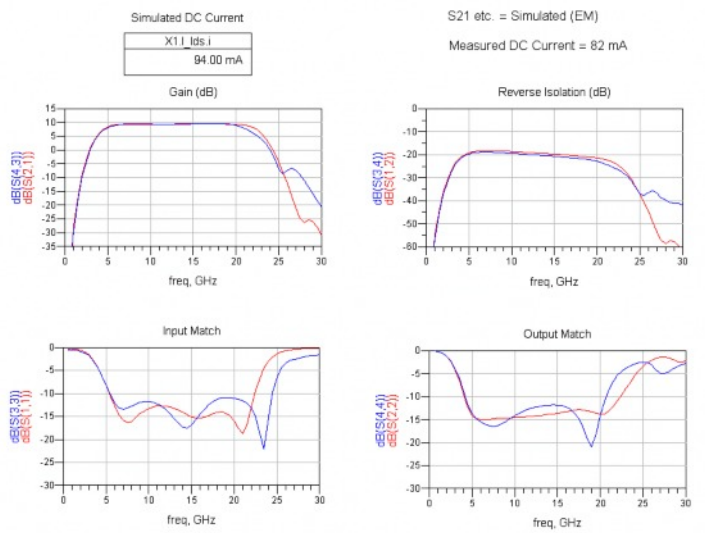


Figure 4: Comparison of measured to simulated s-parameters for the 6 to 18GHz gain block

Power Amplifier MMIC for the 26GHz 5G Pioneer Band

The EU's Radio Spectrum Policy Group (RSPG) recommended the 26GHz (24.25 to 27.5GHz) band as the Pioneer Band for mm-wave 5G in Europe. Figure 5 shows a photograph of a Power Amplifier (PA) MMIC designed by PRFI for 5G applications in this band. It was fabricated on one of WIN Semiconductors' 0.15µm InGaAs pHEMT processes and was optimised for best efficiency when operating backed-off from compression to maintain modulation fidelity. The die size is 3.5mm x 1.2mm with scope for reduction to 3.0mm x 1.2mm using a production mask set.

Figure 6 shows measured to simulated s-parameters, the quiescent bias point is 210mA from 6V. Measured performance is in blue and simulated in red showing the measured gain response (S21) virtually overlaying the simulated. The S11 is below -18dB across the full 26GHz 5G band. The output was matched for best efficiency when operating backed-off from compression but the S22 is still a very respectable -12dB worst case across the full Pioneer Band.

Figure 7 shows the RFOW measured and simulated output power and power added efficiency (PAE) against back-off from P-1dB at 26GHz. The simulated traces use dashed lines and the measured use solid lines. The output power at P-1dB is 26dBm with a PAE of 30%. The measured to simulated PAE is in very good agreement across a wide range of back-off.

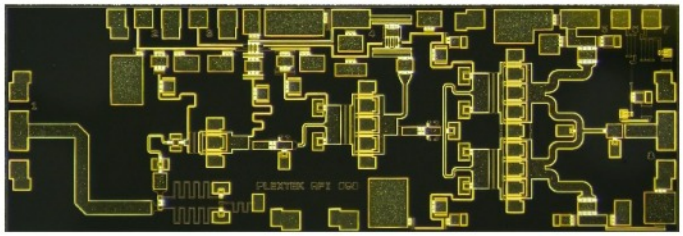


Figure 5: Die photograph of a 26GHz 5G PA MMIC

PRFI Ltd.
The Plextek Building, London Road, Great Chesterford,
Saffron Walden, CB10 1NY, UK

T: +44 (0) 1799 796464 **E:** enquiries@prfi.com **W:** www.prfi.com

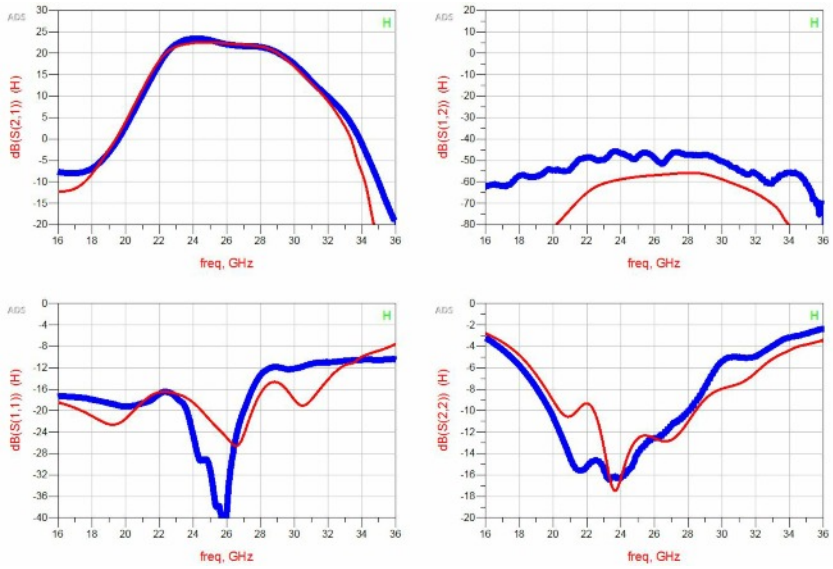


Figure 6: 26GHz 5G PA RFOW measured and simulated small signal response

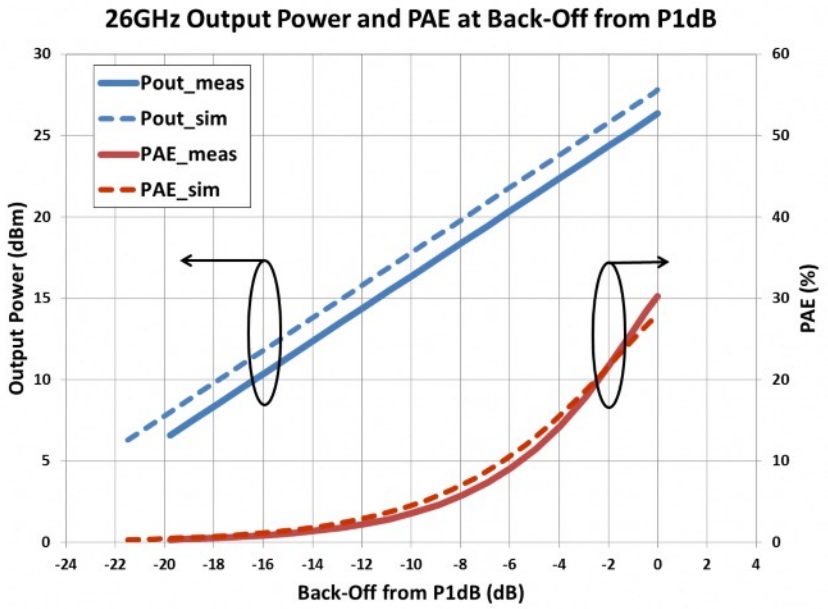


Figure 7: 26GHz 5G PA RFOW measured and simulated power and PAE at 26GHz

6 to 23GHz Double Balanced Mixer

Other areas in which PRFI has significant design expertise include MMIC mixers. One such design is the 6 to 23GHz double balanced mixer shown below in Figure 8. This was designed on Qorvo's 0.13µm PHEMT process, TQP13. It has an RF and LO frequency range of 6 – 23GHz and can operate with IF frequencies in the range of DC - 4GHz. Typical conversion loss is around 7dB with an IIP3 of 22dBm. The LO to RF rejection is excellent at around 45dB.

Figure 9, shows conversion gain when the mixer is configured as a down converter with high side RF, and an LO input power of +15dBm. The measured conversion gain across the RF input range of 6 to 23GHz is within 1dB of simulated with an average value of -7dB. The input referred third order intercept point (IIP3) for the mixer in this configuration is shown in Figure 10; the LO input power was again +15dBm and the tone spacing 10MHz. The average IIP3 across the band is around 22dBm for both measured and modelled and for a given RF frequency the measured IIP3 is typically within 2dB of the modelled.

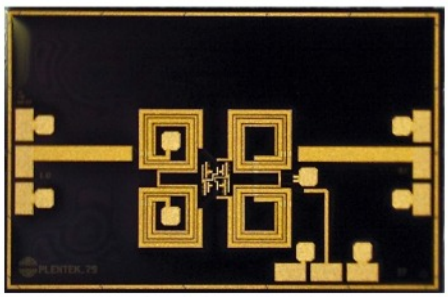


Figure 8: Die photograph of 6 to 23GHz double balanced mixer

PRFI Ltd.
The Plextek Building, London Road, Great Chesterford,
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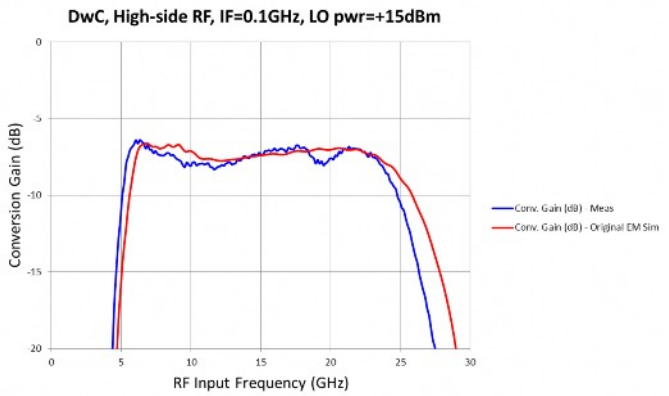

Figure 9: Comparison of measured to simulated conversion gain of 6 to 23GHz double balanced mixer.

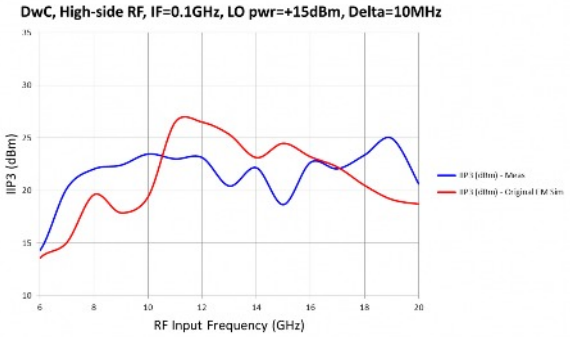

Figure 10: Comparison of measured to simulated IIP3 of 6 to 23GHz double balanced mixer.

20 to 30GHz SPDT Switch MMIC for 5G

The next MMIC to be reviewed is a single pole double throw (SPDT) switch that operates with low insertion loss and high isolation across the 5G bands at 24GHz, 26GHz and 28GHz. It was designed on WIN Semiconductors' 3µm PIN diode process. The die measures 3mm x 1mm and a photograph is shown below in Figure 11. The DC control pads are on the top-side, the common RF port is on the bottom side and the switched RF ports are on the left and right hand sides.

The switch was measured RFOW with the left hand side RF path enabled and the right hand side path disabled. Applying a negative voltage to a path's control pin enables that path (turning the diodes "off" and setting it into its low loss state); applying +3V disables the switch path (turning the diodes "on" and putting that path into its high loss, isolating, state). The on-state switch draws a total of 20mA from the +3V supply. The negative bias on the off-state arm determines the power handling of the switch. A negative bias of -15V allows operation to power levels of +33dBm without significant compression.

A plot showing the measured and modelled S-parameters for the enabled path is given below in Figure 12 showing very low insertion loss (~ 0.66dB) and excellent agreement between measured and modelled. A comparison of the measured and modelled disabled path isolation is given in Figure 13 demonstrating a very high isolation of over 45dB across the 20 to 30GHz operating band.

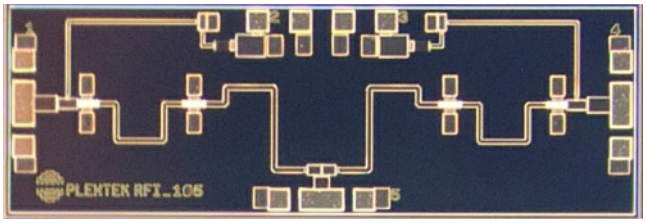

Figure 11: Die photograph of 20 to 30GHz 5G PIN diode switch

PRFI Ltd.
The Plextek Building, London Road, Great Chesterford,
Saffron Walden, CB10 1NY, UK

T: +44 (0) 1799 796464 **E:** enquiries@prfi.com **W:** www.prfi.com

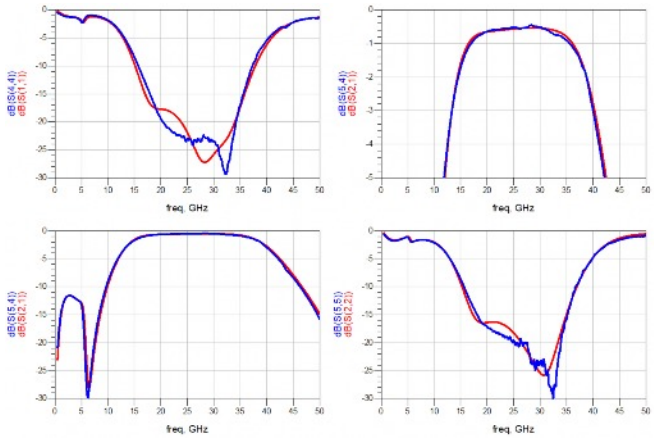

Figure 12: 28GHz 5G PIN switch measured and simulated, enabled path s-parameters

Figure 13: 28GHz 5G PIN switch measured and simulated, disabled path isolation

SMT packaged mm-wave MMICs

The packaging of MMICs into low cost SMT packages eases handling and assembly and is therefore the preferred format for most volume applications. At mm-wave frequencies it is essential that co-design and simulation of the package and MMIC is undertaken as an integral part of the MMIC development process if optimum performance is to be obtained.

PRFI has experience of developing mm-wave MMICs using a range of SMT packaging approaches including over-moulded plastic, air-cavity plastic and custom laminate. With plastic packaging a custom leadframe design is normally used to obtain best RF performance. The laminate approach is inherently a custom design. The transition between the MMIC bond pad and the PCB on which the packaged part is mounted must be modelled and optimised during the design process. The effects of the bondpads, bondwires, PCB and package leadframe must all be accounted for and in the case of over-moulded plastic the moulding compound itself must be incorporated into the EM simulation of the MMIC.

Figure 14 is a photograph of a plastic packaged PA MMIC for the 28GHz 5G band (27.5 – 28.35GHz) mounted on an evaluation PCB. It was designed on a 0.15µm E-mode pHEMT process from WIN Semiconductors and is housed in a 4mm x 4mm over-moulded 20 pin QFN package. A custom leadframe was designed as part of the development process to optimise the RF performance of the packaged part. The PA includes an on-chip temperature compensated power detector and offers a gain of 20dB with a P-1dB of 26dBm and a PAE of 30%. The design was optimised for best PAE when operating with IMD3 products at -35dBc (which was around 7dB back-off). At this operating point a PAE of around 7 to 9% was demonstrated.

The measured to modelled performance of a packaged PA on the evaluation PCB is plotted in Figure 15. A TRL calibration tile was used to reference the measured performance to the ports of the package on the PCB.

A custom laminate package was developed for the 26GHz 5G PA MMIC featured earlier in this paper. The package was a QFN format and housed two MMICs to provide a dual channel component as depicted in the photograph of the evaluation PCB shown in Figure 16.

A comparison of the RFOW measured performance of the PA die to the measured performance of the dual channel packaged component on an evaluation PCB is shown in Figure 17. Both channels of the packaged part are plotted as the solid traces; the dashed traces are the RFOW measured performance. The difference between the RFOW and packaged part performance is modest demonstrating the quality of the RF package design.

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Saffron Walden, CB10 1NY, UK

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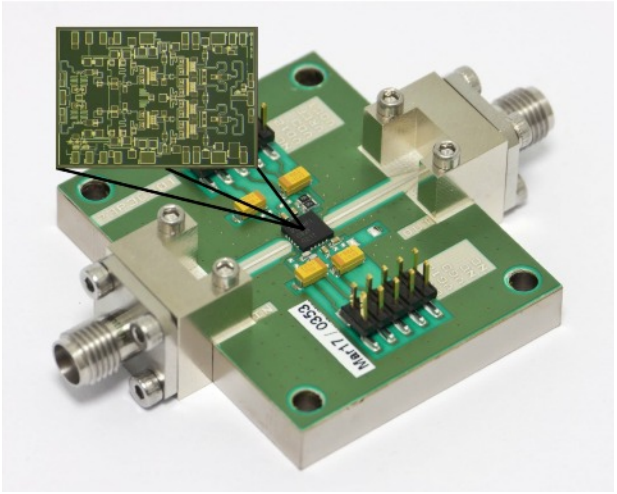

Figure 14: 28GHz 5G PA in 4mm x 4mm over moulded plastic QFN

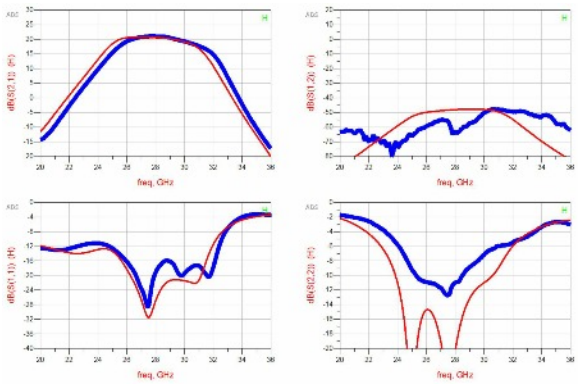

Figure 15: Plastic packaged 28GHz PA for 5G, measured to simulated performance

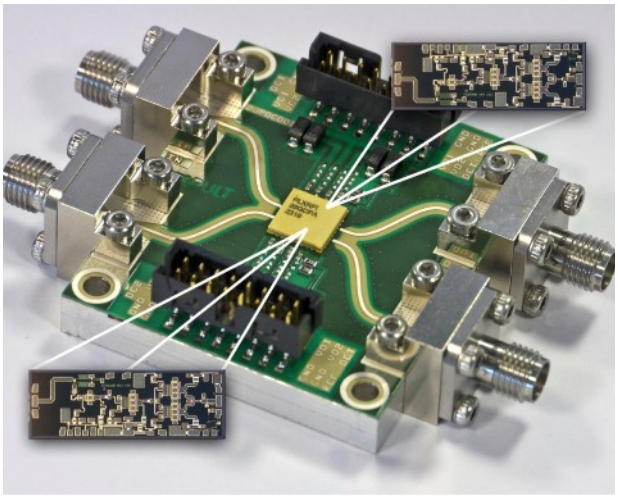

Figure 16: Dual channel 26GHz 5G PA in custom laminate package

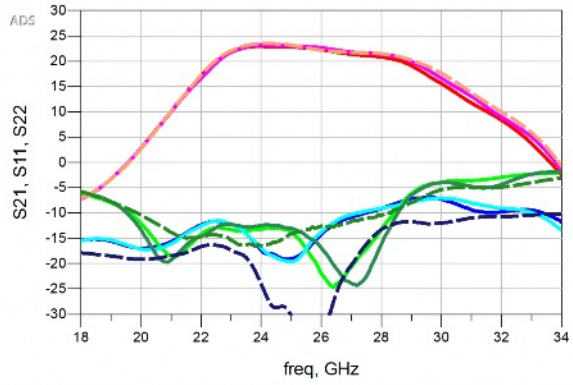

Figure 17: Measured s-parameters of two channels of a packaged PA compared to RFOW

Conclusion

This white paper has given an overview of a proven approach to accurately simulating custom MMICs. A cross-section of recent design work carried out by Plextek RFI has been presented, which demonstrates consistent first pass success through close measured and modelled agreement. Such agreement was presented for a range of circuit functions, operational frequencies and process nodes.

By cultivating a company culture of right first time design success, Plextek RFI has enabled its clients to reduce their product development timescales, cost and risk.

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