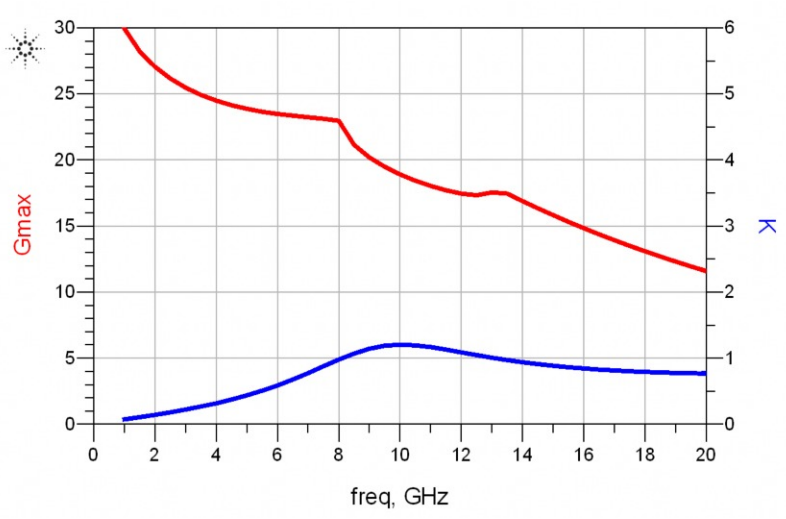
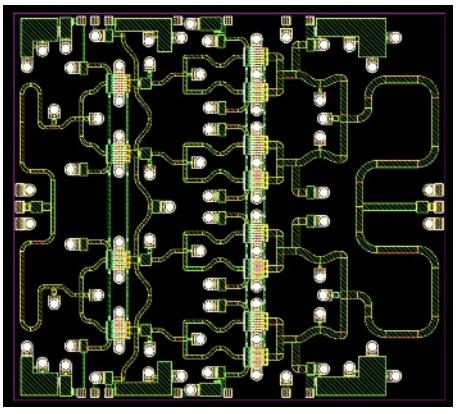
25W X-band GaN PA MMIC Design

This case study describes the design and performance of a 25W X-band GaN PA MMIC designed on WIN's 0.25µm GaN on SiC process. The design has a small signal gain of over 25dB from 10 to 12GHz with a gentle positive gain slope. The saturated output power is over 25W from 10 to 11.5GHz and PAE is over 33%.



Gmax and K of a single GaN transistor



Layout of 25W GaN PA MMIC

Gallium Nitride (GaN) MMIC processes suitable for operation at microwave frequencies are now commercially available from a number of vendors worldwide. The high breakdown voltage of GaN transistors and their ability to operate reliably at high junction temperatures make them well suited to the realisation of high power amplifiers. The design presented here uses the 0.25µm GaN on SiC process from WIN Semiconductor, based in Taiwan.

As the total gate periphery of a transistor increases (unit gate width and/or number of gate fingers) the associated parasitics increase and the high frequency performance degrades. Microwave PA MMICs are therefore best realized by combining multiple transistors of an appropriate geometry. The first stage in the design process is to select the transistor size and bias.

An 8x120µm device was chosen, biased at +28V drain-source voltage (Vds) and a drain-source current (Ids) of 100mA per mm of gate width. The Gmax plot (and stability factor, K) are shown above. It can be seen that over the entire X-band this particular device is unconditionally stable, which is an attractive feature. The transistor has a maximum available gain of >17dB up to 12GHz. Series or shunt resistors can be added to the device input to further improve or broaden in-band stability. As the full PA design develops, these resistors can be reduced (or even removed) as practical implementation losses are introduced.

A load-pull simulation of the device is presented overpage. Here it can be seen that when driven into a load impedance of 16+j.27 Ω (at 10GHz) the device is capable of delivering a maximum power of 4.3W with 45% efficiency.

The next stage of the design process is to proceed with the design of a single stage PA. This single-stage will form the basis of the power combined stages required to deliver the high power levels needed.

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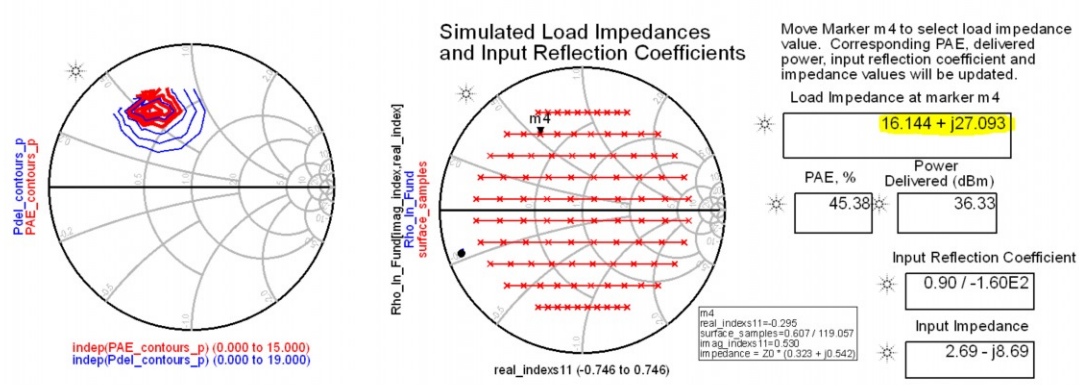


Load-pull simulation for 8x120µm WIN GaN HEMT

The single-stage design utilises a 2-pole low-pass output matching network to match the output of the transistor to the required load impedance for maximum power transfer. An input matching circuit is also added, along with bias tees, decoupling and stabilisation resistors. The small-signal gain, return losses and output power of the single-stage design at 6dB compression are shown below. The amplifier delivers >13dB gain and just less than 4W output power from 10 to 11.5GHz.

For a high power design, the combination of eight transistors in the output stage represents a good choice in terms of trade-off between combining network losses, practical layout approaches and achieving high output power levels. The design approach taken was to develop a two transistor design, then a four transistor design (combing two of the two transistor networks) and finally an eight transistor design by combining two of the four transistor networks.

With multiple power combined transistors loop stability must be considered and appropriate balancing resistors included to suppress the tendency towards odd-mode oscillation. These are easily included in a custom designed MMIC.

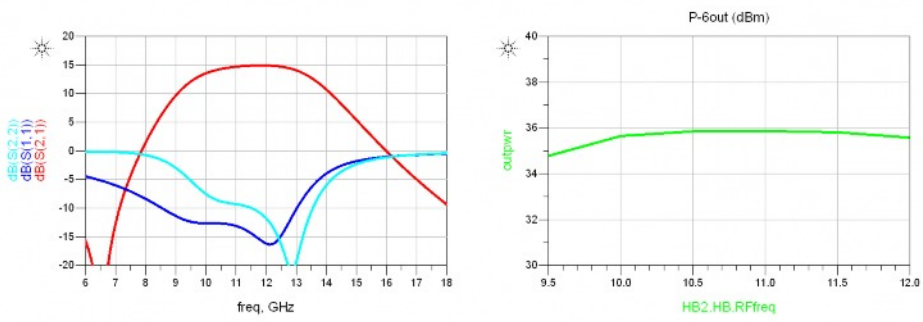
Care must be taken to ensure that the tracks and planned bondwire connections have adequate current carrying capability when operating under large signal drive and for a large PA such as this, the output stage must often have bias applied from both sides of the die. As well as ensuring in-band stability, the designer must also consider out of band stability, particularly at low frequencies where the GaN transistors have very high levels of available gain.

On-chip RC networks at the gate and drain bias points were included to provide additional losses at low frequencies and ensure stability down to below 100MHz. Off-chip de-coupling can be used to provide damping at lower frequencies.

After the basic design of the output stage is completed the driver stage can be designed. Selection of the size of the driver stage is critical. GaN transistors have a soft compression characteristic and if the driver stage is too small the amplifier will need to be driven to very high levels of compression in order to achieve the desired output power levels.

Conversely if the driver stage is too large then Power Added Efficiency (PAE) will suffer. For this design a four transistor driver stage was selected.

The available gain of the GaN transistors is quite high at X-band and the two stage design has over 25dB of gain. The addition of a third stage would have resulted in small signal gain levels approaching 40dB, which was considered too high for a single MMIC at X-band.



Small-signal performance and output power at 6dB compression for the single-stage amplifier

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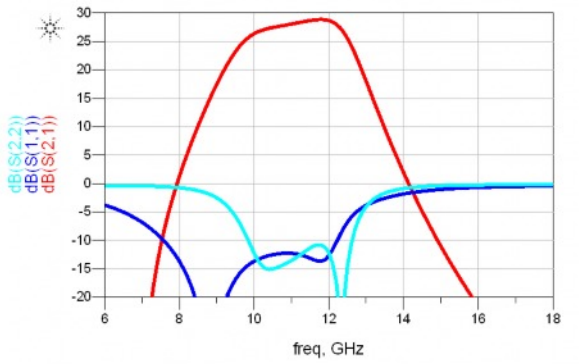
Although GaN transistors are able to withstand high operating temperatures, the thermal design of a GaN PA cannot be overlooked. The thermal conductivity of the SiC substrate is very good (at room temperature around 10 times higher than that of GaAs) but it does reduce significantly with increasing temperature, which means the thermal impedance of GaN MMICs varies with the baseplate temperature. It is the responsibility of the designer to ensure that the junction temperature of the transistors is acceptable at the specified maximum operating temperature.

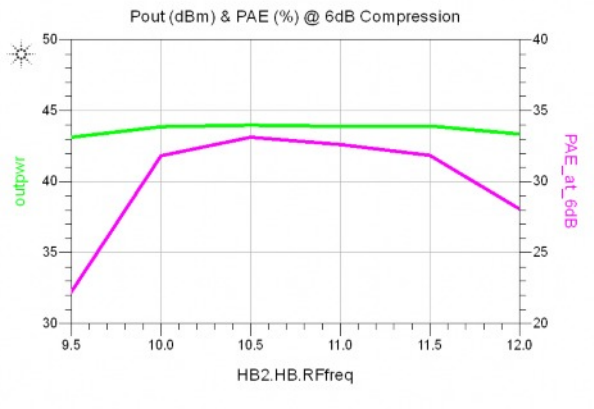
The final small-signal performance of the complete 2-stage amplifier is presented in the top right figure. Across 10 to 12GHz the gain is >25dB, with a useful positive gain slope with frequency. The graph below this shows the output power and power added efficiency (PAE) at 6dB compression. It can be seen that over 10 to 11.5GHz the output power is 25W with a PAE of >33% An input drive level of +24dBm is adequate to reach the 25W output level.

The DC input current verses input power level is shown in the final figure. The nominal quiescent DC bias current is 1.174A, which equates to each of the twelve HEMTs being biased at 100mA/mm of gate width. Obviously the DC current rises with drive level. At 6dB power compression the nominal DC current consumption has risen to the order of 2.75A.

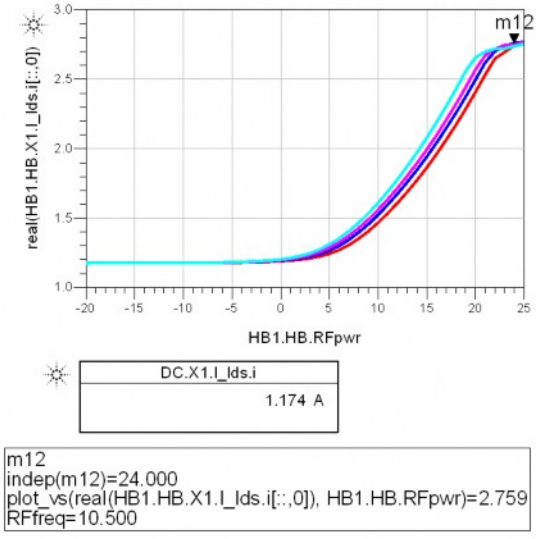
The final GDSII layout of the MMIC PA is shown on the front page. Chip area is 4.8 x 4.4 mm^2.



Final small-signal performance of the 2-stage PA



Output power and power added efficiency at 6dB compression



DC current under large-signal drive conditions

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