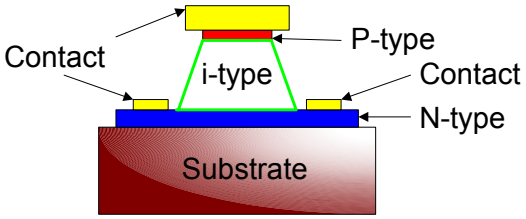
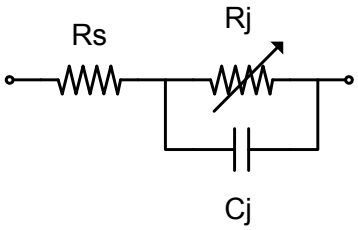
Broadband, Low-Loss Limiter MMICs

Limiters are used to protect receiver circuitry from high power signals (such as nearby transmitters), which could otherwise result in permanent damage. They need to be low loss, as any insertion loss adds directly to the noise figure of the receiver. In many applications small size and weight and broadband operation are also desirable. This technology overview presents PIN diode limiter MMIC designs that meet all of these requirements with an operating band of 0.5 to 20GHz and an insertion loss of less than 0.55dB. A method of increasing the maximum input power level to around 20W CW is presented. The die size is just 2.03mm x 0.72mm.



Cross-section of an integrated PIN Diode



Electrical equivalent model of a PIN diode

PIN diodes are a popular technology choice for limiter circuits because a small device is able to handle relatively large amounts of power. They are available as discrete components which are frequently used to realise limiter modules. PIN diodes are also available on IC processes; this results in reduced circuit parasitics and facilitates the design of broadband, low-loss components. The limiter IC designs presented here use TriQuint's Vertical PIN diode (VPIN) process.

A PIN diode takes its name from its structure; it comprises a region of high resistivity 'Intrinsic' material sandwiched between regions of P-type and N-type semiconductors, as depicted in the cross-section above. When the PIN diode is forward biased, charge carriers are injected into the I region lowering its resistance. Thus at RF and microwave frequencies a PIN diode behaves as a current controlled resistor, and can be configured to make excellent RF/microwave switches.

The electrical equivalent circuit for the intrinsic PIN diode is shown above. It includes a parasitic capacitance (Cj) in parallel with the junction resistance (Rj). This affects the high frequency behaviour of the diode and must be accounted for in the design process. The electrical model for a packaged PIN diode would also include package parasitics, which can be avoided with an integrated design.

When configured as a limiter, PIN diodes are normally mounted in shunt to ground. When high power RF signals are present, charge carriers are injected into the I region of the diode on one half cycle and removed on the opposite polarity half cycle. Imperfections in the I region and statistical considerations mean an accumulation of charge develops in the I region, thereby reducing the diode's resistance. This charge generation also results in a DC current (a rectified portion of the RF signal) which must have a DC return path in order for the limiter to function correctly.

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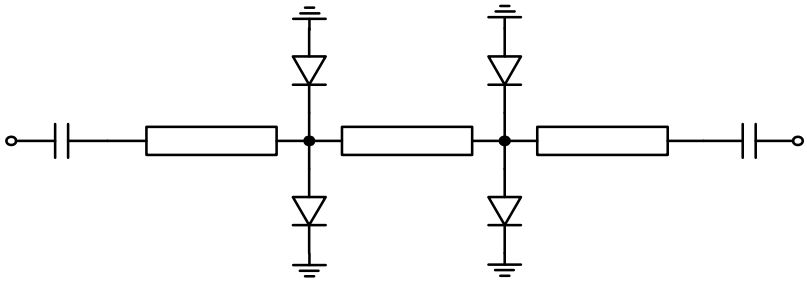


Schematic of the symmetrical 5th order limiter

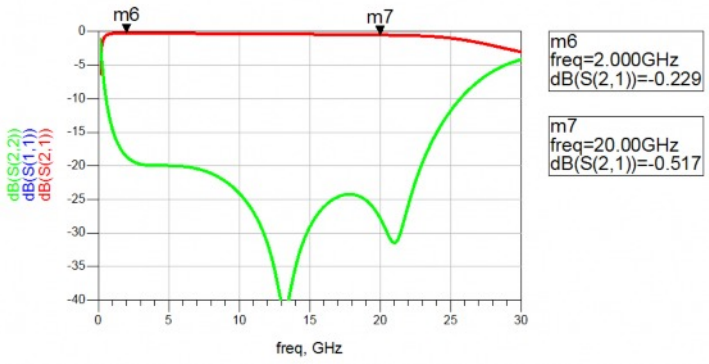
Limiter Design and Simulation:
The design methodology adopted with the limiters presented here was to use pairs of antipodal (back-to-back) shunt mounted diodes. This approach inherently includes a DC return and avoids the need for a broadband RF choke. The parasitic capacitance of the zero-biased back-to-back diode pairs was absorbed into a low-pass filter structure to allow a broadband design that covered the desired 0.5 to 20GHz operating band. This conveniently allows multiple stages of shunt diode pairs to be incorporated into the design, which then provides limiting to slightly lower power levels than with just a single diode pair. It also provides a convenient stepping stone to increasing the power handling.

A schematic of the basic limiter (which was based on a 5th order low-pass filter) is shown above. The two pairs of back-to-back PIN diodes replace the shunt capacitors in the low-pass filter. High impedance (narrow) metal tracking is used to implement the series inductors of the filter. On-chip DC blocks (MIM capacitors) are included at both the RF input and output.

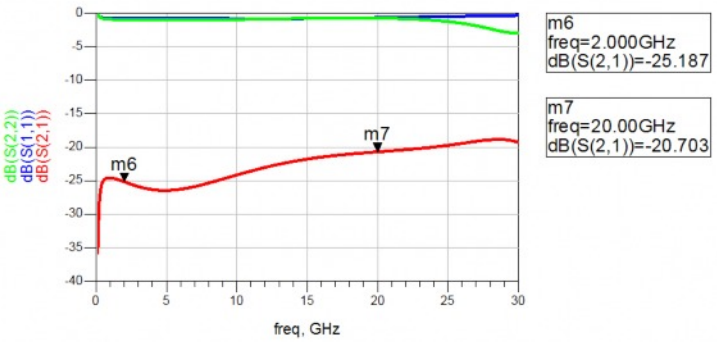
The small-signal simulated S-parameters of the basic symmetrical limiter are shown below. The results include practical bondwire inductance at the input and output ports. All transmission line structures are EM simulated.

Return loss is greater than 18dB above 2GHz but degrades a little at low frequencies to 13dB at 500MHz. This is a result of the practical size limitations of the on-chip DC blocks.

When a high level RF signal is incident on the limiter, the effect is to turn on the diodes as the RF biases them into forward conduction. This effect can be understood by changing the small-signal model for the two front-end diodes from the zero-bias state to a +1.25V/5mA forward conduction state. The resulting performance is shown in red in the plot below and indicates that, under large RF signal drive, the limiter should limit the signal breaking through by the order of 20 to 25dB. Simulations using large- signal PIN diode models provide an improved means of simulating the effect and are presented later.



Small-signal low loss performance of the symmetrical 5th order limiter



Small-signal "attenuating" performance of the symmetrical 5th order limiter

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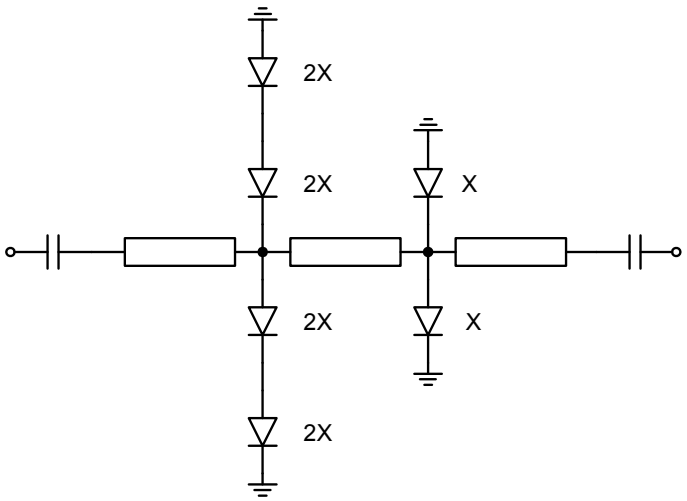
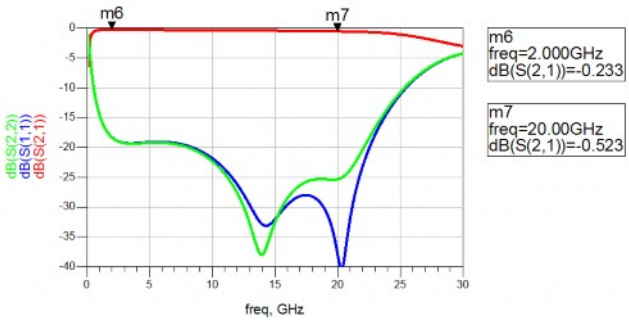


Schematic of the high-power (asymmetrical) 5th order limiter



Small-signal low loss performance of the high-power (asymmetrical) 5th order limiter

Increasing power handling

The power handling capability of the limiter is set by the size (area) of the first diode pair. When an RF signal is present, forward current will flow in these diodes, which will increase with increasing RF power. The current handling capability of the diodes, and so the RF signal handling capability of the limiter, is set by their area. The symmetrical 5th order limiter described above should be able to withstand a CW input power in the region of 5W.

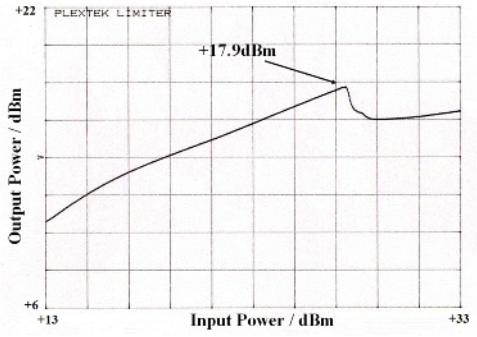
In order to increase the power handling capability of the limiter a second, asymmetrical topology was developed. This is shown in the schematic above. The main change is that each of the first antipodal pair of shunt diodes is replaced by a cascade of two diodes. These are set to be twice the area so that the two in cascade have twice the current handling capability and the limiter can handle 6dB more input power, around 20W CW. Capacitance, however, is nominally unchanged and so the achievable RF performance should be very similar.

The small-signal simulated S-parameters of the high-power asymmetrical limiter are shown above. As before it includes practical bondwire inductance at input and output and all transmission line structures are EM simulated. The small-signal RF performance is actually extremely similar to that of the lower power symmetrical limiter presented above with just a very slight degradation in return loss and a tiny increase in insertion loss.

Large-signal modelling of the limiters

Accurate large-signal modelling of PIN diodes is problematic, and the foundry does not provide large-signal models for the PIN diodes. However, PRFI implemented a large-signal model based on the measured performance of previous limiter designs fabricated on the TriQuint VPIN process. The plots over page show the simulated power transfer characteristics of the two limiters. The three traces show performance at 2GHz, 10GHz and 18GHz. It can be seen that the difference with frequency is relatively modest. The saturated output power level is around 17 to 18dBm.

It should be noted that practical limiters designed on this process have a more complex power transfer characteristic with a pronounced "kink" where the output power falls back after reaching a peak, as shown in a measured performance plot below. The large signal model does not predict this kink but it does predict the correct peak output power level.



Measured Pin versus Pout from a previous PRFI limiter design

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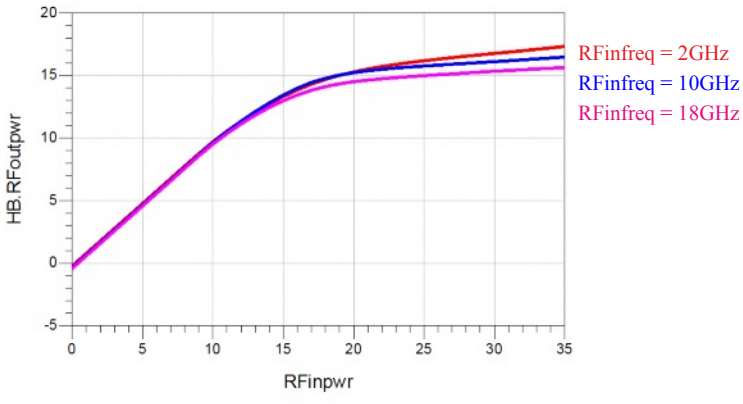
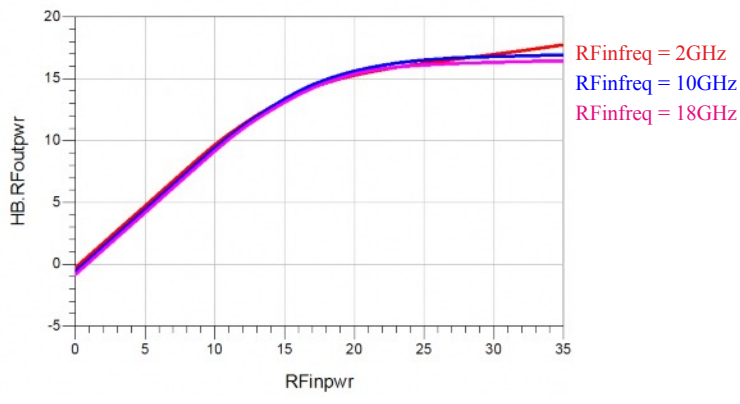


Pin versus Pout of the symmetrical 5th order limiter at 2, 10 and 18GHz

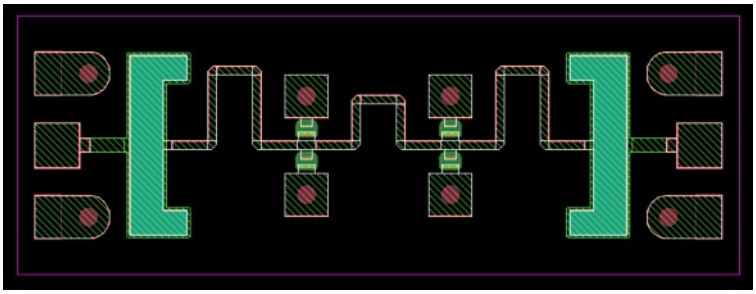


Pin versus Pout of the high-power (asymmetrical) 5th order limiter at 2, 10 and 18GHz

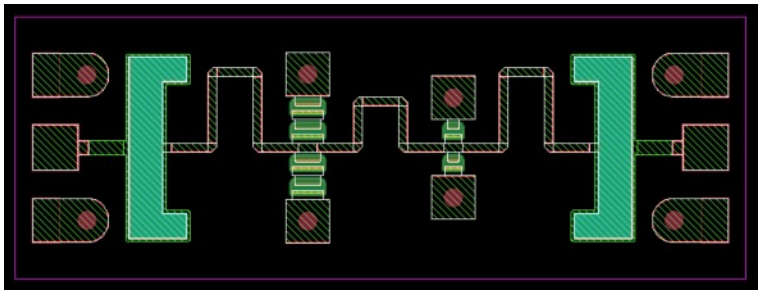
Layout:

Layout plots of both limiters are shown below.

Die area is identical for each IC at just 1.46 mm^2.



Layout of the symmetrical 5th order limiter



Layout plot of the high-power (asymmetrical) 5th order limiter

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