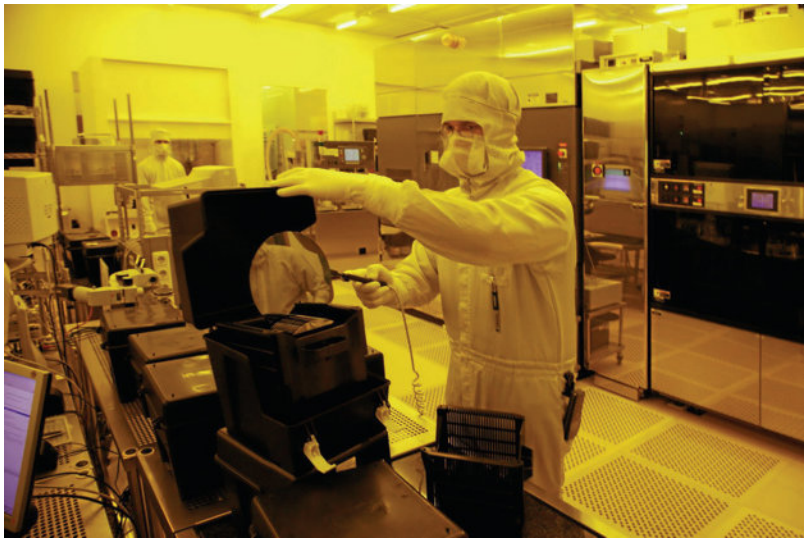
Technology Overview

mmWave SiGe IC Design

Increasing consumer demand for high data-rate wireless applications has resulted in development activity to exploit the mm-wave frequency range where large amounts of spectrum are available. The ISM band around 60GHz (V-band) and the light-licensed spectrum at E-band (71-76GHz and 81-86GHz) are of particular interest. Whilst commercial mm-wave ICs have traditionally been realised using III-V based processes, the increasing availability of SiGe processes with very high Ft's offers an alternative solution benefiting from the potential for lower unit costs in volume production.



Preparation and Processing of SiGe wafers in the IHP Pilot Line (Courtesy R.Weisflog/IHP)

SiGe technology uses HBTs (heterojunction bipolar transistors) to provide impressive transistor performance to high mm-wave frequencies. One of the main features of the SiGe HBT that allows superior performance compared to a Si BJT is a base with a graded Ge concentration. The resulting transistors have higher β, higher ft and fmax and lower NFmin making the more advanced SiGe processes suitable for mm-wave applications.

A number of vendors now offer SiGe processes on a commercial foundry basis that are suitable for the realisation of circuits operating at V-band and E-band. Access to very high Ft SiGe processes embedded in 250nm or 130nm BiCMOS technologies is available through IHP GmbH. The photograph above shows the preparation and processing of SiGe wafers in the IHP pilot line.

Whilst transistors with adequate Ft are a necessary requirement for the development of Si mm-wave ICs, there are many other issues that complicate the design process and must be adequately addressed. These include:

- Substrate losses
- Grounding inductance
- Breakdown voltage (which reduces with increasing Ft)
- Thermal issues (e.g. self heating, particularly when biased for highest Ft)

This technology overview investigates the realisation of analogue circuits for V-band and E-band applications using appropriate IHP SiGe processes. It considers the design of amplifiers as a vehicle for assessing the achievable performance, the implementation issues and appropriate design approaches. It considers process selection, device and bias selection and the choice of circuit architecture required to demonstrate strong performance at mm-wave frequencies.

PRFI Ltd.
The Plextek Building, London Road, Great Chesterford,
Saffron Walden, CB10 1NY, UK

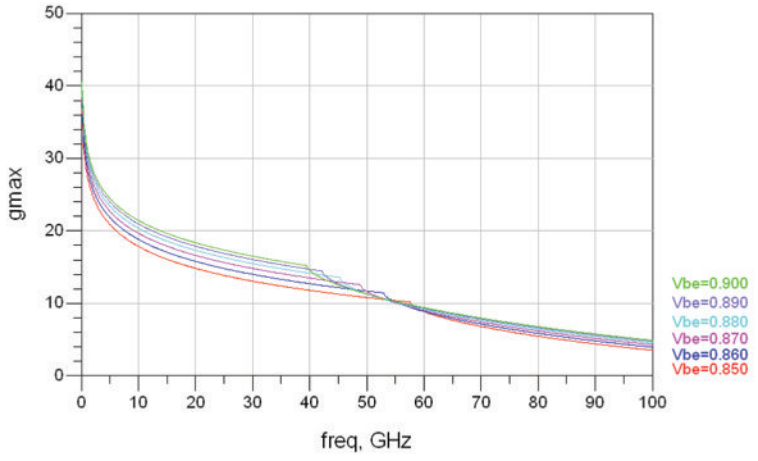
T: +44 (0) 1799 796464 **E:** enquiries@prfi.com **W:** www.prfi.com

V-band IC Design

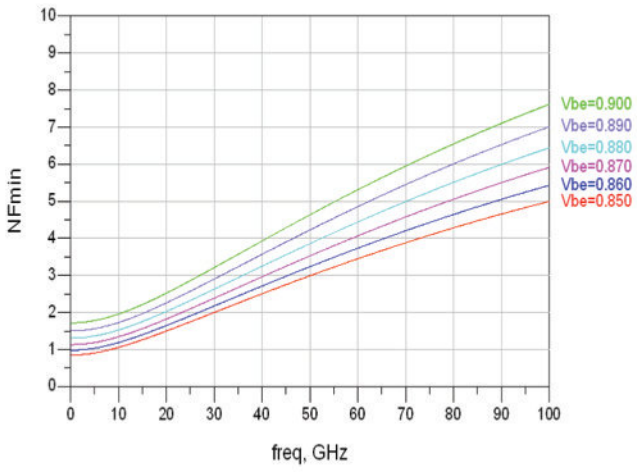
Process Selection: When considering the design of mm-wave Si circuits it is tempting to select the process with the highest available Ft. However considerations such as breakdown voltage, cost and current consumption led to the selection of the SG25H3 process for V-band operation. It is a 0.25µm technology, which features high performance npn HBTs offering a good compromise between breakdown voltage (BVCEO = 2.3V) and high frequency operation (ft/fmax = 110/180 GHz respectively).

Bias Point: For peak Ft the current density of the high performance npn HBTs on this process is around 6mA/µm^2. However, simulations of Gmax and NFmin as a function of collector current density (curves of varying Vbe in the plots below) were carried out to gauge the bias point that would allow a suitable trade off of gain with noise figure. Plots of Gmax and NFmin, as a function of Vbe, for a device in common emitter configuration, are shown below. At this stage zero emitter grounding inductance was assumed. A Vce bias of 1.7V was used to optimise linearity. The emitter area is 0.22 x 6.72µm^2.

The selected bias point was a collector current density of 3mA/µm^2, corresponding to a typical Vbe of 0.87V, as this offers a good compromise between Gmax and NFmin. The choice of Vce bias of 1.7V was made considering linearity, voltage swing and device breakdown voltage. Under these quiescent conditions, the HBT dissipates 5.1mW/µm^2 which is relatively low and performance degradation due to thermal issues is less of a concern. This allows the HBT, of a given emitter area, to be implemented with fewer parallel devices (a lower value of M) and hence reducing associated interconnect parasitics introduced in layout.



Gmax versus frequency for different bias points, SG25H3 transistor



NFmin versus frequency for different bias points, SG25H3 transistor

PRFI Ltd.
The Plextek Building, London Road, Great Chesterford,
Saffron Walden, CB10 1NY, UK

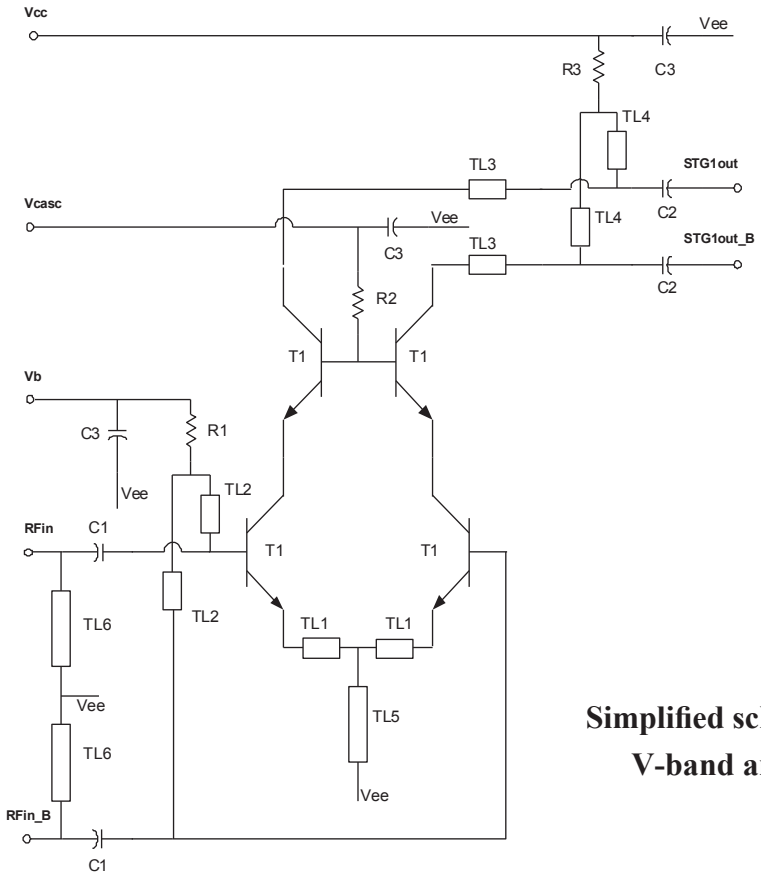
T: +44 (0) 1799 796464 **E:** enquiries@prfi.com **W:** www.prfi.com

The selected device in common emitter configuration is unconditionally stable above 49GHz at the chosen bias point. This is evident from the kink in the Gmax characteristic at this frequency showing where the device moves from a region of potential instability to a region of unconditional stability. Being unconditionally stable across the band of interest (57 to 65GHz) is an attractive feature as stabilising circuitry would need to be added to a conditionally stable device, which would cause a drop in gain.

V-band Amplifier Architecture:
Assuming the amplifier is to be used in a real application then the practical issues of assembly and packaging must be considered from the outset. The expected grounding inductance in particular can be problematic. Regardless of the approach taken to minimise grounding inductance it will still be significant at mm-wave frequencies. Overlooking this will at best result in an amplifier with lower gain and most likely an unstable amplifier. Interestingly many publications on mm-wave SiGe amplifiers ignore this inductance choosing to only mention performance when measured on an RFOW probing station which provides an effective grounding inductance approaching zero.

Packaging and assembly of V-band and E-band ICs is a complex matter in its own right and a detailed discussion of the subject is beyond the scope of this text. However, consideration has been given to providing tolerance to a reasonable level of grounding inductance. The design was therefore progressed with the assumption that the grounding inductance due to assembly/packaging could be as high as 50pH which is realistic for processes without low inductance through vias.

A differential architecture benefits from a virtual earth and was selected to provide tolerance to the grounding inductance. It also provides rejection of common mode signals and has other advantages including improved second harmonic performance and higher dynamic range.



Simplified schematic elements of V-band amplifier 1st stage

PRFI Ltd.
The Plextek Building, London Road, Great Chesterford,
Saffron Walden, CB10 1NY, UK

T: +44 (0) 1799 796464 **E:** enquiries@prfi.com **W:** www.prfi.com

V-band Amplifier Stability: Although the use of a differential topology means that the grounding inductance no longer has any effect on the wanted signal, it is still very significant in common mode and can cause instability. During the design of the amplifier, measures were taken to ensure stability in differential mode, common mode and mixed mode for all frequencies up to the Fmax of the transistors, for a grounding inductance of up to 50pH.

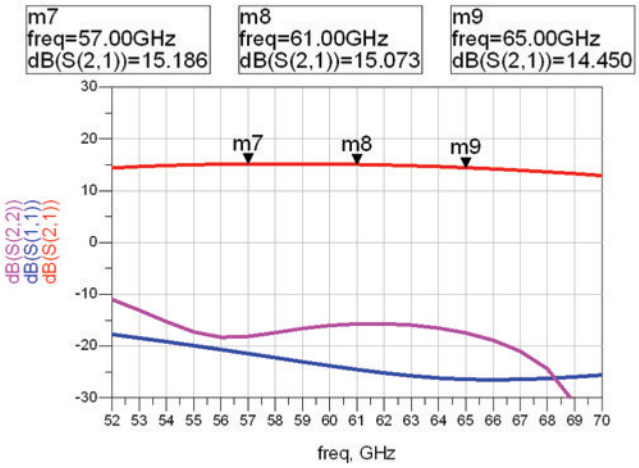
A cascode architecture was adopted for the amplifying transistors. This has several benefits for mm-wave amplifiers implemented on SiGe including increased voltage handling, reduced Miller capacitance and higher isolation between input and output making impedance matching easier and improving stability.

To achieve adequate gain a two stage design was progressed, each stage comprising a cascode transistor arrangement. All devices were biased at 3mA/μm^2, with the devices in the second stage having twice the emitter area as those in the first. This approach ensures an adequate drive ratio between the stages which is required for linearity.

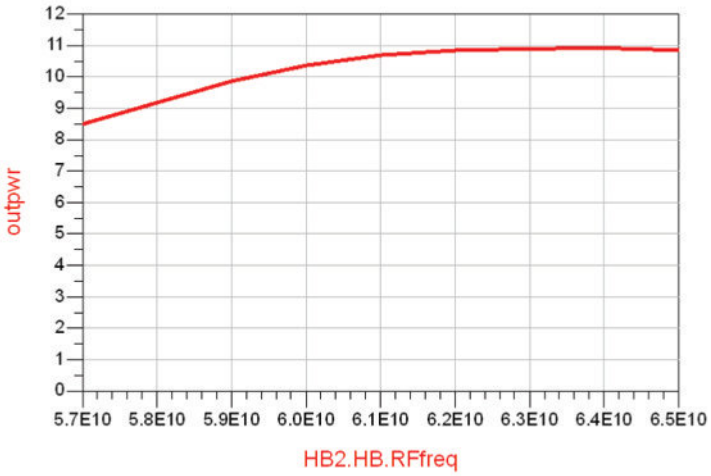
V-band Amplifier Schematic:
A simplified schematic showing the main elements of the 1st stage of the V-band amplifier is depicted on the previous page. All components are from the SG25H3 Process Design Kit (PDK). The design makes good use of micro-strip transmission lines which use a lower metal layer (metal 1) as the ground plane and an upper metal layer (top metal 2) as the conductor. Substrate losses are minimised by connecting the metal 1 ground plane to the substrate with an adequate number of p-taps in the layout.

In this design the microstrip lines are essentially being used as low value inductors. Note the use of a length of microstrip line in the tail of the differential pair which helps to increase common mode rejection. The tail current source, traditionally used to bias differential amplifiers, was avoided as this can lead to common mode stability problems.

Series resistors are used in the bias paths. These only affect common mode signals and in fact contribute to providing common mode rejection and ensuring stability. The bases of the common base stage of the differential cascode are joined to form a virtual earth. Stage 2 uses a very similar topology as stage 1 with the addition of matching circuitry to transform the output impedance to 50Ω. The overall 2-stage amplifier runs off a 3.3V supply and draws a total quiescent current of 24mA.



Small signal performance of V-band amplifier



Output P1dB of V-band amplifier

PRFI Ltd.
The Plextek Building, London Road, Great Chesterford,
Saffron Walden, CB10 1NY, UK

T: +44 (0) 1799 796464 **E:** enquiries@prfi.com **W:** www.prfi.com

V-band Amplifier Performance: Typical V-band amplifier simulated performance is shown above, the small signal gain is 14.8dB ±0.4dB across the band 57 to 65GHz. The output return loss is better than 15dB across the band and the input return loss is better than 20dB. The output power at 1dB gain compression is 9.5dBm ±1dB.

E-band IC Design

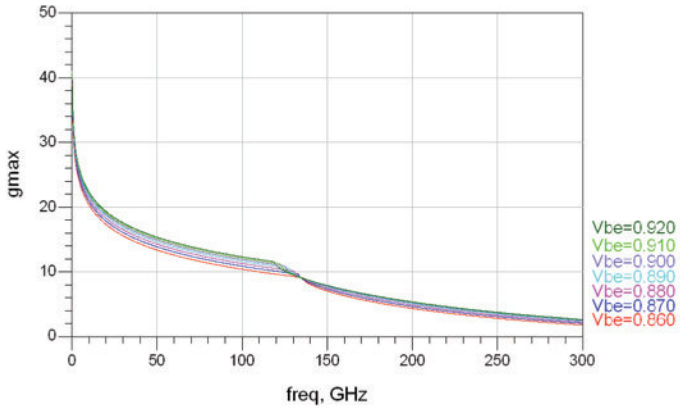
Process Selection: Although SG25H3 demonstrated good performance at V-band, IHP's higher Ft processes were considered more appropriate for an amplifier working at E-band, (71 to 86GHz). After due consideration the selected process was SG13G2 which is a high performance 0.13µm technology. This offers an npn HBT with very high frequency performance (Ft/Fmax = 300/500GHz) with a slightly lower breakdown voltage (BVCEO = 1.7V).

Bias Point: For peak Ft the current density for this device is around 30mA/um^2, however, simulations of Gmax and NFmin as a function of bias were carried out to gauge the bias point that would provide the best trade-off of gain for noise figure at E-band. Plots of Gmax and NFmin, as a function of Vbe, for a device in common emitter configuration with Vce = 1.2V are shown below. The emitter area is 0.07 x 7.2um^2.

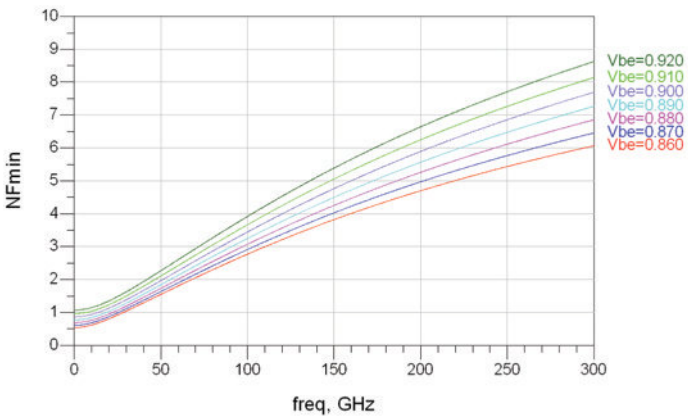
A current density of 14mA/µm^2 was selected (corresponding to a typical Vbe of 0.88V) as providing a good compromise between Gmax and NFmin.

The choice of Vce bias of 1.2V was made considering linearity, voltage swing and device breakdown voltage. Under these quiescent conditions, the HBT dissipates 16.8mW/µm^2 which is a higher power density than that of the transistors of the V-band amplifier (5.1mW/µm^2) and requires the HBT to be implemented with a higher number of parallel devices in layout.

The 0.07 x 7.2µm^2 emitter area device is potentially unstable at E-band so gain must be sacrificed in order to ensure stability. As the Gmax for this device at the chosen bias point is sufficiently high at the top of the band (12dB at 86GHz) this reduction in gain can be afforded.



Gmax versus frequency for different bias points, SG13G2 transistor



NFmin versus frequency for different bias points, SG13G2 transistor

PRFI Ltd.
The Plextek Building, London Road, Great Chesterford,
Saffron Walden, CB10 1NY, UK

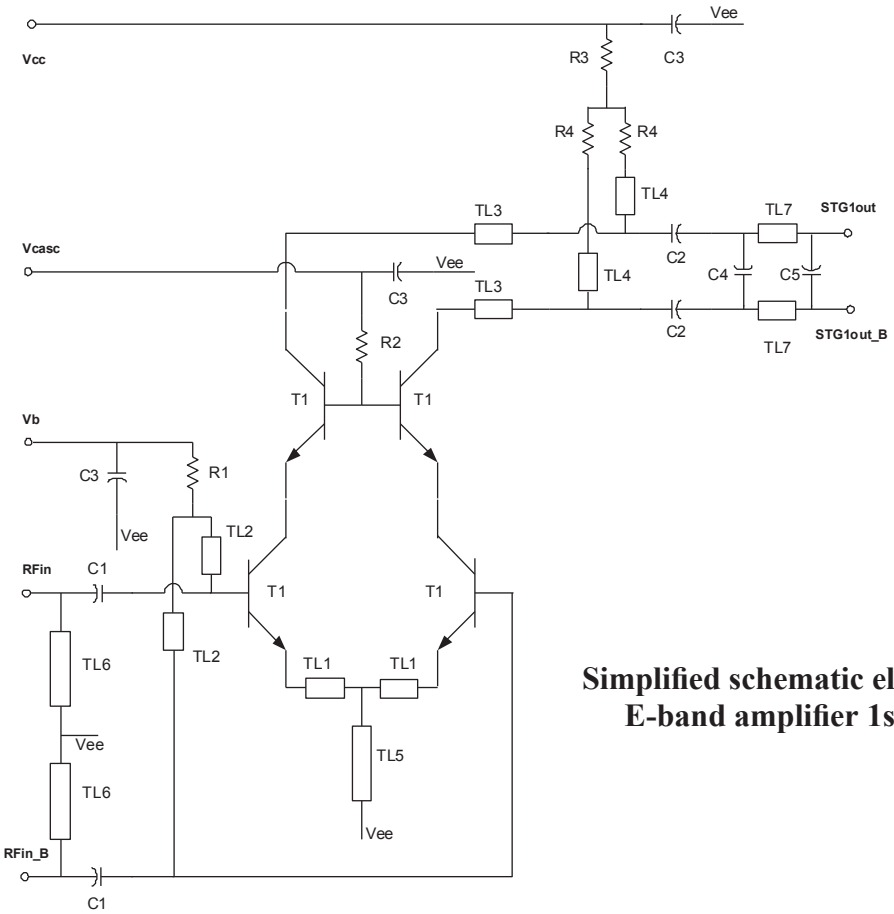
T: +44 (0) 1799 796464 **E:** enquiries@prfi.com **W:** www.prfi.com

E-band Amplifier Architecture:
As for the V-band amplifier, the E-band amplifier was assumed to have to tolerate 50pH grounding inductance. This should provide sufficient tolerance for assembly and/or packaging in a real application. A similar two stage cascode architecture was adopted using a differential topology. All devices were biased at 14mA/μm², with the devices in the second stage having twice the emitter area as those in the first. As before, this is to ensure an adequate drive ratio between the stages which is required for linearity.

E-band amplifier Schematic:
A simplified schematic showing the main elements of the 1st stage of the E-band amplifier is depicted below. All components are from the SG13G2 PDK. The use of the same architecture as the V-band design means that the design incorporates many similar features including the use of micro-strip transmission lines and series resistors in the bias paths. In the E-band design, however, extra loss was required differentially in the output match by means of resistors R4. As well as stabilising the stage, this loss allows for a good wideband impedance match. Although not strictly necessary, it was convenient to match the output of stage 1 to 50Ω. Stage 2 uses a very similar topology to stage 1.

The E-band amplifier runs off a 2.5V supply and draws a total quiescent current of 42mA. It is stable in differential mode, common mode and mixed mode for all frequencies up to Fmax, for up to 50pH of grounding inductance.

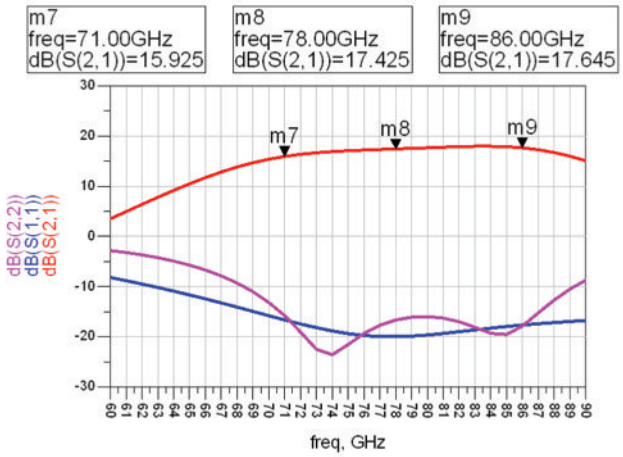
E-band Amplifier Performance:
Typical E-band amplifier simulated performance is shown on the following pages. The small signal gain is 16.8dB ±0.9dB across the band 71 to 86GHz and it exhibits a slight positive gain slope which is often a desirable feature. The output return loss is better than 16dB across the band and the input return loss is better than 17dB. The output power at 1dB gain compression is 7.5dBm ±1dB across the band. Noise figure is between 4dB and 4.25dB across the band.



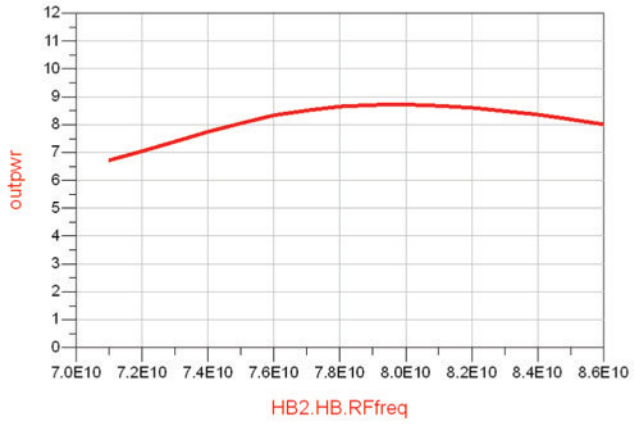
Simplified schematic elements of E-band amplifier 1st stage

PRFI Ltd.
The Plextek Building, London Road, Great Chesterford,
Saffron Walden, CB10 1NY, UK

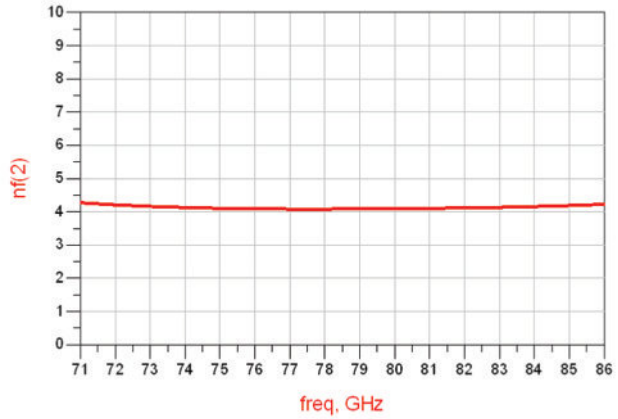
T: +44 (0) 1799 796464 **E:** enquiries@prfi.com **W:** www.prfi.com



Small signal performance of E-band amplifier



Output P-1dB of E-band amplifier



Noise Figure of E-band amplifier

Summary and Concluding Remarks:

This technology overview has reviewed the use of SiGe technology for the realisation of mm-wave ICs. It has considered V-band and E-band amplifiers designed on IHP's SiGe processes to explore the implementation issues and assess the achievable performance. Issues such as substrate loss, grounding inductance, breakdown voltage and thermal performance become more problematic at high mm-wave frequencies.

These issues were addressed during the design through appropriate choice of process, bias point and circuit architecture. It is noted that the potential problems that practical levels of grounding inductance, resulting from assembly and/or packaging, can cause are often inadequately covered in existing literature. The designs presented are tolerant to grounding inductances of up to 50pH, which is considered as a realistic level for a practical implementation and mandates the choice of a differential architecture.

It is also vitally important to ensure amplifier stability in differential mode, common mode and mixed mode. After careful consideration of the main implementation issues, this overview has demonstrated that strong performance at mm-wave frequencies can be achieved using IHP's SiGe processes.

PRFI Ltd.
The Plextek Building, London Road, Great Chesterford,
Saffron Walden, CB10 1NY, UK

T: +44 (0) 1799 796464 **E:** enquiries@prfi.com **W:** www.prfi.com