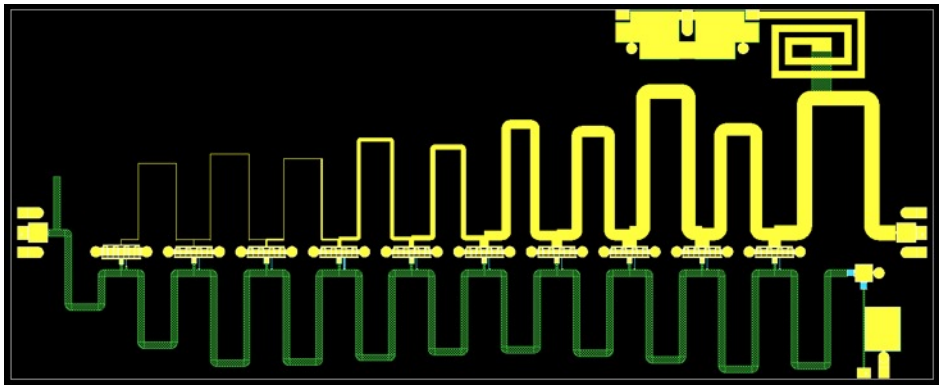
Case Study

Broadband (2-18GHz) GaN PA Design

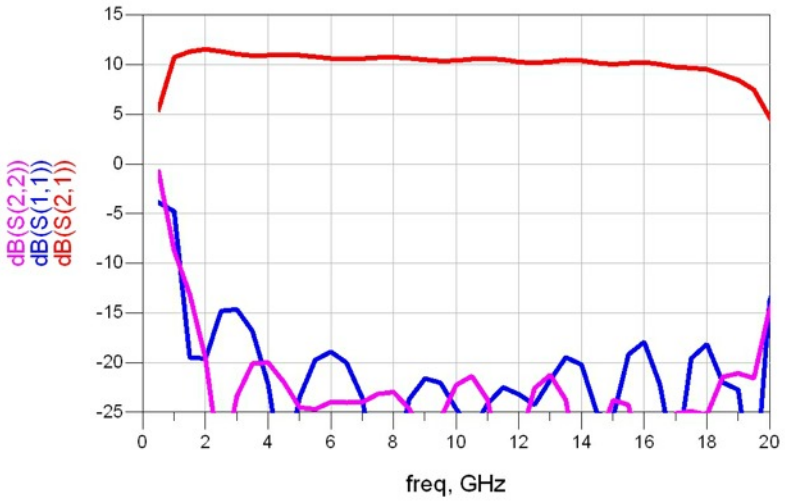
GaN technology can be used to realise broadband microwave power amplifiers with output power levels of around 5 times those of the best performing GaAs PHEMT parts. This case study presents details of a 2-18GHz GaN PA MMIC with a gain of 10dB and an output power capability of 7W.



GDSII Layout of the 2-18GHz GaN PA

Gallium nitride (GaN) processes with transistors suitable for operation at microwave frequencies are now commercially available from a number of foundries. The higher breakdown voltage and maximum junction temperature of GaN transistors make them well suited to the realisation of high power amplifiers. The design presented here is a Non-uniform Distributed Power Amplifier (NDPA), which allows simultaneous coverage of the entire 2-18GHz band with high output power and flat gain.

The design makes use of the 0.25µm gate length GaN on SiC process of TriQuint Semiconductor. The distributed topology embeds multiple transistors within low pass filter structures. The gate and drain capacitances of the transistors form the shunt capacitive elements of the filters. A total of ten transistors have been used to give an output power of around 7W over 2 to 18GHz. The NDPA design approach is to taper the characteristic impedance of the drain line so as to try and maintain a near optimum load impedance at each transistor.

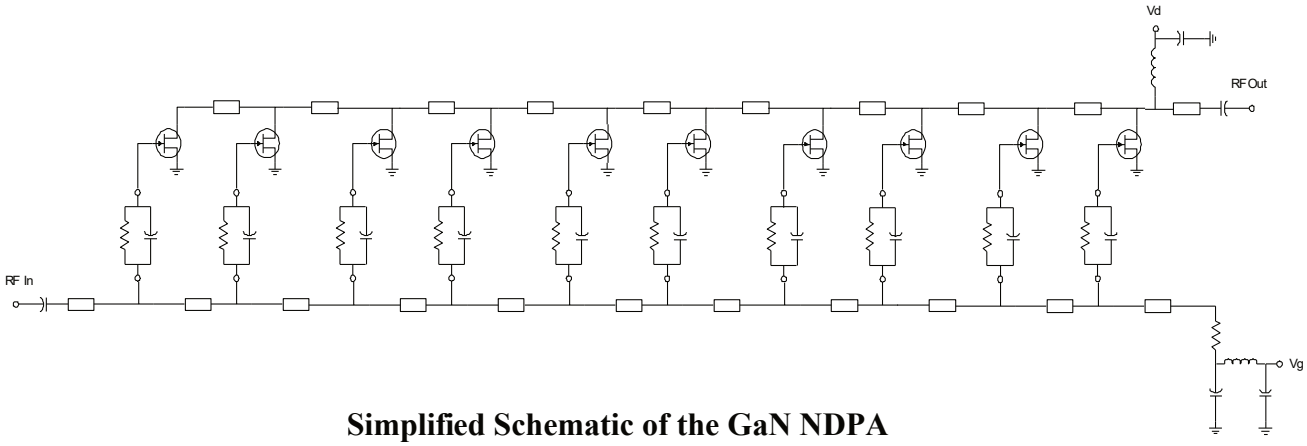


Small-signal Performance

Sheet Code 0625

PRFI Ltd.
Abbey Barns, Suite 1, Building 3
Duxford Road, Ickleton, Cambridge, CB10 1SX, UK

T: +44 (0) 1799 796464 **E:** enquiries@prfi.com **W:** www.prfi.com



Simplified Schematic of the GaN NDPA

A simplified circuit schematic of the amplifier is shown above. It can be seen that series capacitors are included at the gate of each transistor. This allows the cut-off frequency of the gate line filter to be increased for a given transistor size so increasing the available output power for a particular upper operating frequency.

The downside to this technique is that some available gain must be sacrificed resulting in a trade-off of gain versus power. The value of the series capacitors is tapered along the gate line to maintain a constant drive level at each transistor input. Gate bias feed resistors are required in parallel with each series gate capacitor.

Careful design of the drain bias choke is essential. The tracks must be wide enough to carry the peak drain bias current and it must have a high enough inductance to present an adequate impedance at the low end of the operating band. The approach adopted here is evident in the amplifier layout plot shown overleaf.

Large-signal Performance

PRFI Ltd.
Abbey Barns, Suite 1, Building 3
Duxford Road, Ickleton, Cambridge, CB10 1SX, UK

T: +44 (0) 1799 796464 **E:** enquiries@prfi.com **W:** www.prfi.com