How to Design a GaN PA MMIC

This white paper describes how to design a custom GaN PA MMIC using a commercially available GaN-on-SiC foundry process. It uses an X-band PA requirement as the design example, and runs through the design process step-by-step to the point of having a completed MMIC layout ready for manufacture. It commences with selection of the most appropriate GaN MMIC process then moves on to transistor level simulations including load-pull analysis to determine the optimum impedances at both fundamental and harmonics. This leads on to the detailed schematic design and MMIC layout methodology. Finally the approach for performing electromagnetic (EM) simulation and layout optimisation is described.

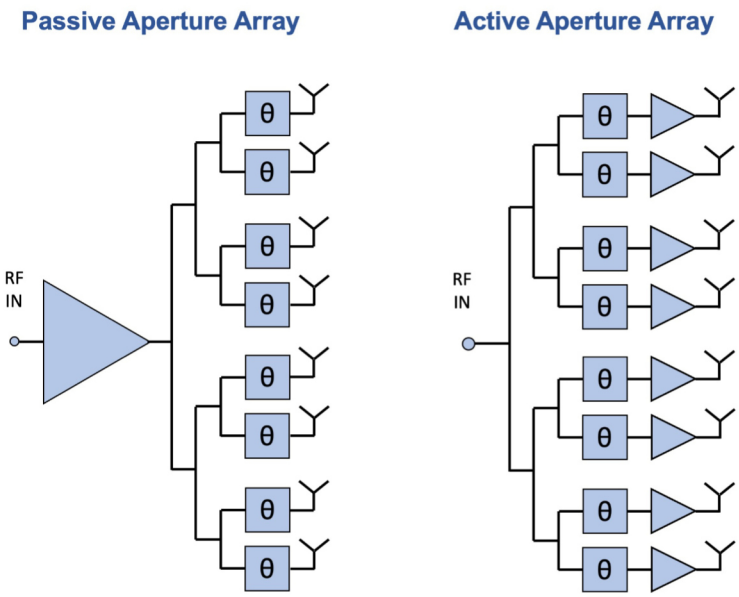

Figure 1: Active phased array radars need a solid-state PA for each element

PA application

The example PA used to illustrate the design process is an X-band (8 – 12GHz) PA for a phased array radar application. X-band radar applications include weather surveillance radar, military radar, and those used for air-traffic control. Increasingly these are active aperture phased array radars, for which multiple solid-state PAs are needed, as shown on the right-hand side in Figure 1. The active array approach enables the radar to position the beam much more rapidly using electronic steering rather than traditional mechanical steering, and can generate multiple independent beams.

There may be hundreds or even thousands of elements in an active phased array, so even a small improvement in PA efficiency or a reduction in size and weight will have a massively beneficial effect on the performance of the entire system. Realising the PA as a GaN MMIC offers advantages in all of these areas.

Advantages of GaN-on-SiC

GaN-on-SiC has become the technology of choice for high-power solid state amplifiers. In addition to high power density and high efficiency, using GaN devices in a PA also enables operation at a high voltage, which means that it can be matched to higher output impedances compared to other device technologies such as GaAs. This means that matching networks can be simpler, reducing transmission line losses. The higher voltage also means that they can operate at lower current levels, reducing I^2R losses. The power density of GaN is four to five times higher than that of GaAs, which means that the MMICs can be smaller, resulting in a compact, lightweight final design with good reliability. The SiC substrate has high thermal conductivity, making it easy to remove heat from the

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Parameter	Target	Units
Frequency	9.0 – 11.0	GHz
SS Gain	25	dB
P_{4dB}	40	dBm
	10	W
PAE at P_{4dB}	> 30	%
Input Return Loss	> 10	dB
Operating conditions	28	V

Table 1: Example PA specification for phased array radar application

device, and allows the device to operate at higher channel temperatures for the same mean time to failure (MTTF).

Design steps

The design begins with the selection of the process and then moves onto device level simulations, selecting the transistor unit cell size, the bias point, and the load and source impedances. This preliminary transistor analysis data is then used to determine the number of stages needed to meet the specification, the number of transistors in the output stage, and the ratio between the driver transistor(s) and the output transistors. From here, the detailed schematic design can be performed with optimisation of bias networks and matching networks. A preliminary layout can then be produced from the schematic design and EM simulations are conducted to optimise and finalise the design. The layout is run through a design rule checker (DRC) to make sure that the foundry will be able to fabricate the design.

Specification and process selection

Table 1 gives a top level specification for a PA, which was used as the design example. The amplifier requires a 2GHz bandwidth centred on 10GHz, with a target small-signal gain of 25dB. For a phased array radar application, the power amplifier is run highly compressed, so the output power is specified at 4dB compression with a target of +40dBm and power added efficiency (PAE) of greater than 30%. Input return loss should be better than 10dB, and the operating voltage is set at 28V.

Selecting the most appropriate MMIC process for the intended application is very important if optimum PA performance is to be obtained. The maximum operating frequency of the process, the required gain, operating voltage and power density must all be assessed. Another consideration is to ensure that the Process Design Kit (PDK) models for the transistors and passive components provided by the foundry are valid and accurate over the required frequency range so that the final PA will give a good agreement with the simulation.

Having established that GaN-on-SiC is very well suited for the planned application, and for microwave PAs in general, there are a number of commercially available processes that could be considered. For this design the Wolfspeed V5 process was selected. Table 2 summarises the process capabilities; GMAX and power density figures are quoted at 30GHz and will be significantly better at 10GHz. The MTTF (Mean Time To Failure) is quoted as 10^6 hours at 225°C. To achieve the

Requirement	G28V5
Maximum operating frequency	F_{MAX} > 120GHz
G_{MAX}	12dB gain @ 30GHz
Power density	3.75W/mm @ 30GHz
Reliability	1x10^6 hours at 225°C
Operating voltage	28V
Device Model Usage	10-28V, 10-300mA/mm

Table 2: Wolfspeed V5 process capability overview

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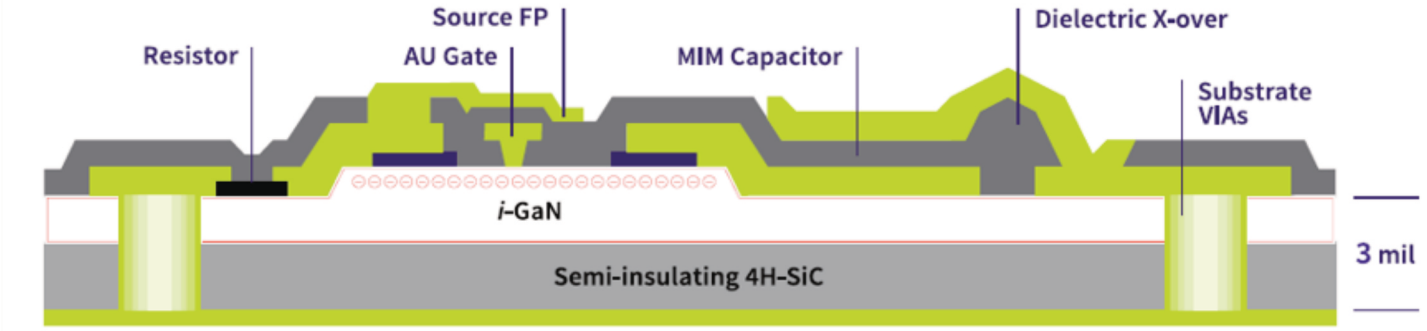

Figure 2: Wolfspeed G28V5 GaN-on-SiC process

same reliability from a GaAs device it would need to be running at about 150°C, so there is a significant advantage in using GaN-on-SiC for this application, as it reduces the cooling requirements of the radar system. The availability of device models that are valid between V_{DS} values of 10V and 28V and 10 – 300mA/mm means that simulations can be carried out over a wide range of bias conditions with the confidence that the resulting MMIC will be 'right first time' and that its measured performance will be well-represented by the design simulations.

A cross-section of the V5 process is depicted in Figure 2. It has a 0.15µm gate length and breakdown voltage of 84V, an RF power density of 3.75W/mm at 30GHz, and a SiC substrate thickness of 75µm. The process offers the standard MMIC passive components (resistors, MIM capacitors and through-hole substrate vias) and benefits from the high thermal conductivity SiC substrate.

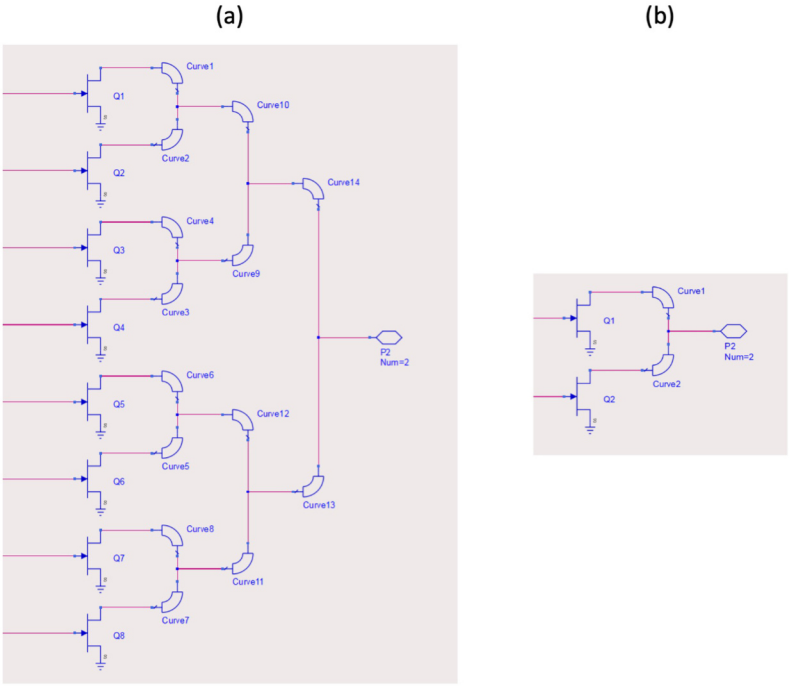

Figure 3: (a) GaAs PA versus (b) GaN PA power combining to achieve required power

GaAs vs GaN-on-SiC

The inherent performance advantages of GaN-on-SiC also help to simplify power combining. Figure 3 compares the circuit required on GaAs with the equivalent on GaN-on-SiC to achieve the same 10W power output. The GaAs IC would require eight transistors, with a complex arrangement of transmission lines to combine the power, which adds loss. In contrast the GaN-on-SiC design requires only two transistors, reducing loss and increasing PAE and making it easier to pass the bias evenly to the transistors. Because there are fewer loops, there is less chance of odd-mode instabilities occurring. It also clearly results in a MMIC with a much smaller die area, which simplifies the design process and gives a higher probability of a 'right first time' design.

Design Approach

Having decided on a suitable process, device-level simulations can begin. The V5 transistors have high gain and are

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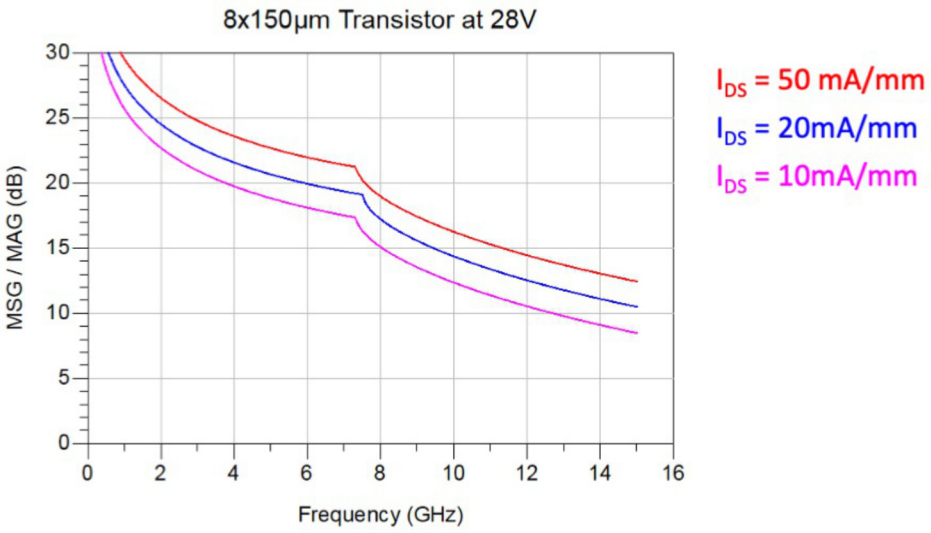

Figure 4: Quiescent bias selection

conditionally stable at X-band. At the outset of the design process it is normal to introduce resistive losses at the transistor input to ensure that the transistor is unconditionally stable across the desired operating band, plus some guard band. The resistive losses can be reduced as the detailed design progresses and practical losses of matching and combining networks are introduced. Stability at lower frequencies must also be addressed as the design progresses, often during the design of the bias network. It is also important to confirm unconditional stability at frequencies above the operating band.

To select the optimum unit gate width, different sizes can be compared. Transistors with shorter unit gate width will benefit from higher available gain but will have a lower output power. The selection of the most appropriate transistor size is one of the likely early steps in designing a microwave PA. The transistor needs to be small enough to provide adequate gain but large enough to allow the desired output power to be achieved by the combination of a practical number of transistors.

The quiescent bias of the transistor impacts the small signal gain, the power transfer characteristics and the linearity. These different performance requirements must be considered when deciding on the optimum bias point. Figure 4 shows the maximum available gain for an 8 x 150µm transistor at 28V V_{ds} with the bias current increasing from 10mA/mm up to 50mA/mm. The effect of the quiescent bias on the gain compression can be evaluated using load pull simulations at a later stage.

Thermal considerations

Because of the high power density in GaN-on-SiC it is very important to ensure that the heat can be dispersed efficiently. The silicon carbide substrate is an excellent thermal conductor, with a conductivity of around 450W/mK, which is around three times that of silicon and nine times that of GaAs. The thermal conductivity is however temperature-dependent, so as it heats up it becomes less efficient at removing the heat. Although this happens in other semiconductor materials, it is more pronounced in SiC, so this needs to be taken into consideration.

The die-attach material, usually solder or silver loaded epoxy, used to attach the MMIC to the package or module is also important thermally. Not only does it need to have good thermal conductivity, but the bond line thickness needs to be kept as small as possible, and attention needs to be paid to avoid gaps in the die attach material after assembly, a phenomenon known as voiding.

It is also necessary to consider the thermal impact of the package and for SMT packaged parts the PCB. Keeping the transistor's operating temperature as low as possible improves the reliability of the amplifier.

One advantage of designing for radar applications is that the PA will generally be operating in pulsed mode, perhaps with a 10% duty cycle, which means that less heat needs to be dissipated than with CW operation. However, as pulse widths get longer, the thermal conditions tend towards those of CW operation. Thermal resistance still needs to be kept low to reduce pulse droop – the phenomenon where the output power drops off towards the end of the pulse due to heating effects, which can affect the radar performance.

Transistor size selection

Small-signal device-level simulations are performed to evaluate available gain in the intended operating band. For this design these simulations resulted in the selection of an 8 x 150µm transistor with intra-source vias at an IDS of 20mA/mm, 28V bias point. The

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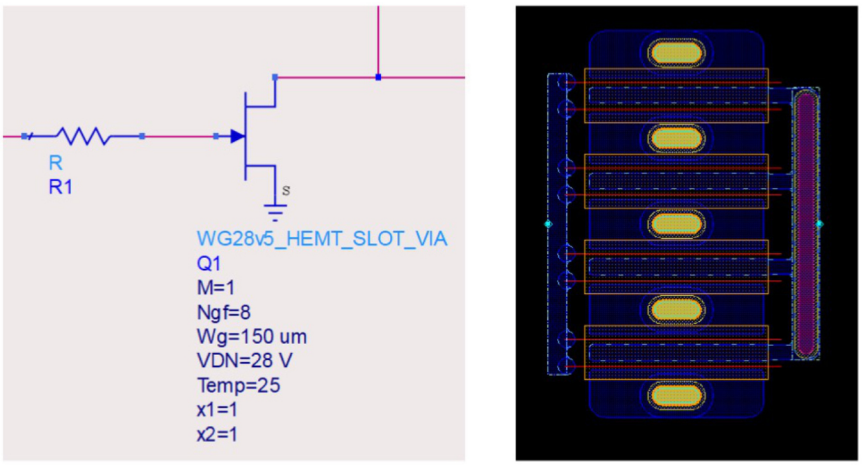

Figure 5: Transistor size selection

layout of the transistor is shown on the right in Figure 5, and it can be seen that the intrasource via style of transistor has vias in between the pairs of gate fingers. The yellow ovals represent the vias and the thin red lines show the gate fingers. There is a pair of gate fingers with a via either side. Spacing out these pairs of gate fingers means that they are further apart, which has thermal advantages. Having more vias reduces the electrical inductance, which is also favourable for the performance. An alternative layout is an edge via layout, where the gate fingers are evenly spaced and there are only two vias - one on either side. Although this layout is slightly more compact, it is not quite as good thermally. For this design the slightly larger intra-source transistor was selected.

Load pull

The next stage of the design process is to carry out load pull simulations to determine how the selected transistor size performs under large-signal operation. Within Keysight ADS there is a standard test bench for transistor load pull. It has the advantage of being easy to set up, but it is also flexible, so it is possible to tune the harmonics and set the conditions to drive the transistor into a suitable mode of operation.

The area of the Smith Chart over which to perform the load pull is first specified, and the number of impedance points to simulate is chosen as a balance between simulation time and accuracy. It is also important to ensure the transistor is driven far enough into compression, as this is where it is intended to be used in its end application, but it must not be driven too hard as this might cause simulation convergence issues. It can sometimes require some optimisation to get the balance right.

Figure 6 shows the load pull simulations at 9GHz, which result in a set of contours that can be used to determine the optimum impedances for PAE, output power and gain. In practice a compromise between these three parameters is selected as the design impedance. The control panel allows the selection of the input power that corresponds to the desired gain compression, and then the optimum impedance as well as the performance figures can be read off. In this particular simulation the transistor is delivering almost 7W output power

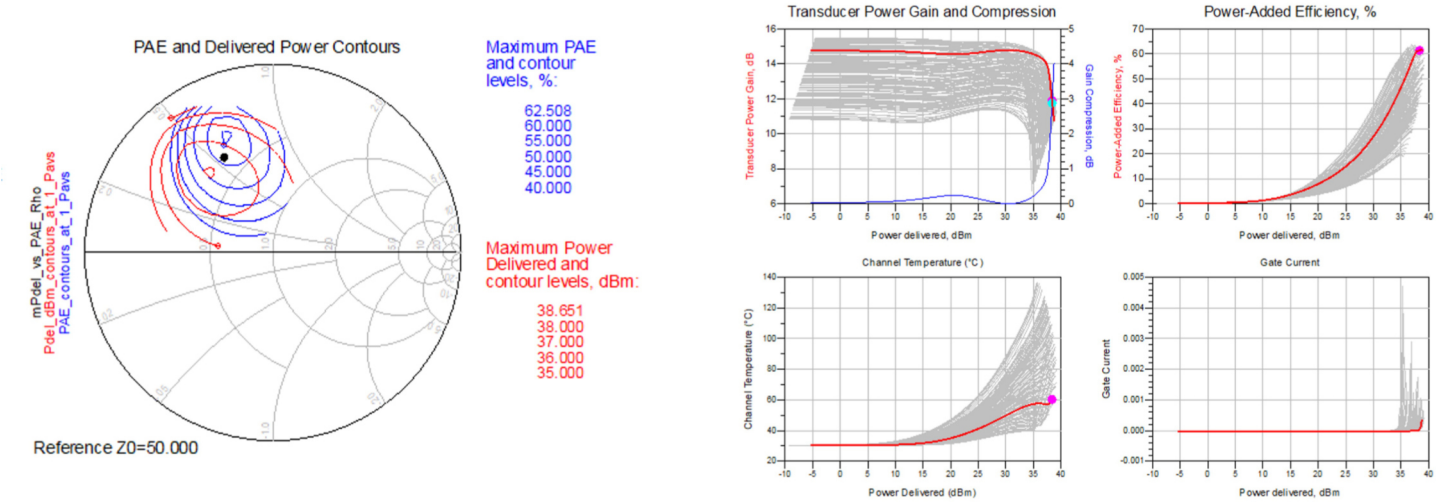

Figure 6: Load pull simulations at 9GHz

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with an efficiency of around 60%. It should be noted that this is the performance for the transistor alone, so it does not include any matching network or power combining losses or the impact of the driver stage. The overall efficiency of the PA will therefore be lower than that shown.

The simulation also allows the gain compression to be inspected. The gate current and the drain current can also be examined to look at the effects on the power supply design. The reason for simulating at different frequencies is to see how these impedances shift with frequency – one challenge of designing matching networks is to try to present the optimum impedance at each frequency, and so this is something that becomes increasingly difficult the greater the design bandwidth. Load pull plots were also produced at 10GHz and 11GHz. At 11GHz the optimum output impedance is between 15Ω and 20Ω. This is much higher than an equivalent GaAs transistor delivering the same power.

Further load-pull simulations can be run across a variety of different operating conditions but in this case these simulations give us enough information to assess the number of transistors needed at the output as well as the required number of gain stages.

Harmonic Load-Pull

The harmonic impedances must also be considered, particularly if the PA is operating heavily into compression. To optimise power and efficiency harmonic tuning of the load can be considered, and to do this the phase of the second harmonic is swept around the edge of the Smith chart. This is shown on the left of Figure 7a for a fundamental frequency of 10GHz; these simulations can of course be repeated for other frequencies. The effect of second harmonic load on power and PAE is shown on the right of Figure 7a. At a phase of 0°, corresponding to an open circuit, the PAE (in red) is just less than 60% and the delivered power (in blue) is around 38.3dBm. Both power and efficiency can be increased by tuning the second harmonic to around 120°, but care is needed to avoid the region around 150° where there is a dramatic dip in power and efficiency. It is also worth remembering that any second harmonic tuning implemented on the MMIC should not adversely affect the fundamental load.

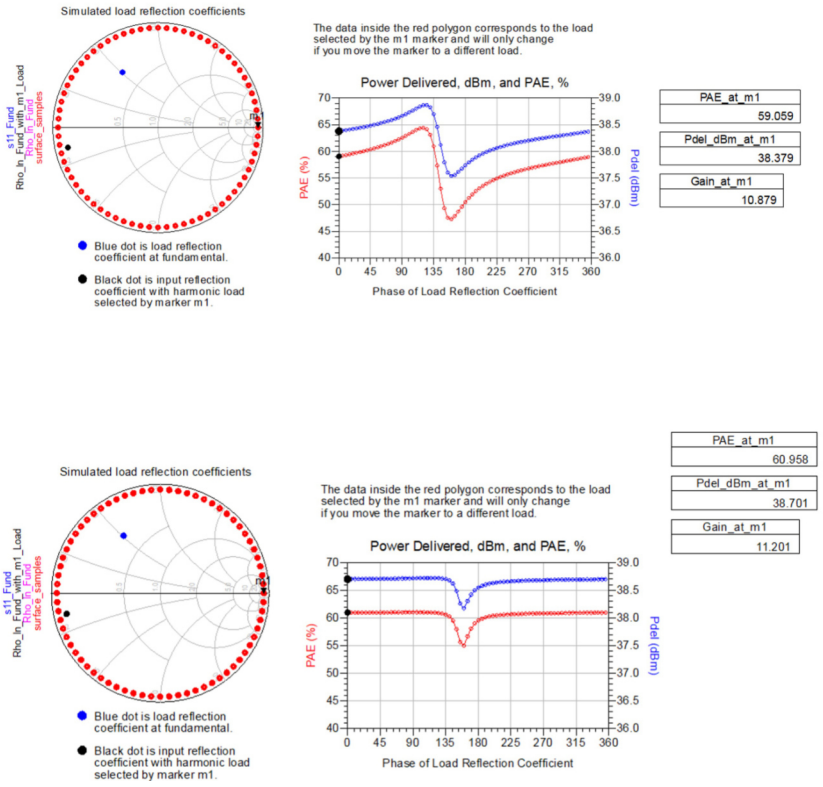

Figure 7(a), top: Second harmonic load pull, and (b), bottom: Third harmonic load pull

The effect of the third harmonic impedance on the power and efficiency can also be simulated, as shown in Figure 7b. Unlike the second harmonic, there is not much performance advantage to be gained by tuning the third harmonic, but the performance dip around 150° needs to be avoided.

PA Topology Considerations

After the device level simulations, the topology of our PA can be determined. By estimating the gain per stage using GMAX simulations and the losses associated with the matching networks, splitting and combining networks and any other relevant components such as gain flattening networks, we can work out how many gain stages are required.

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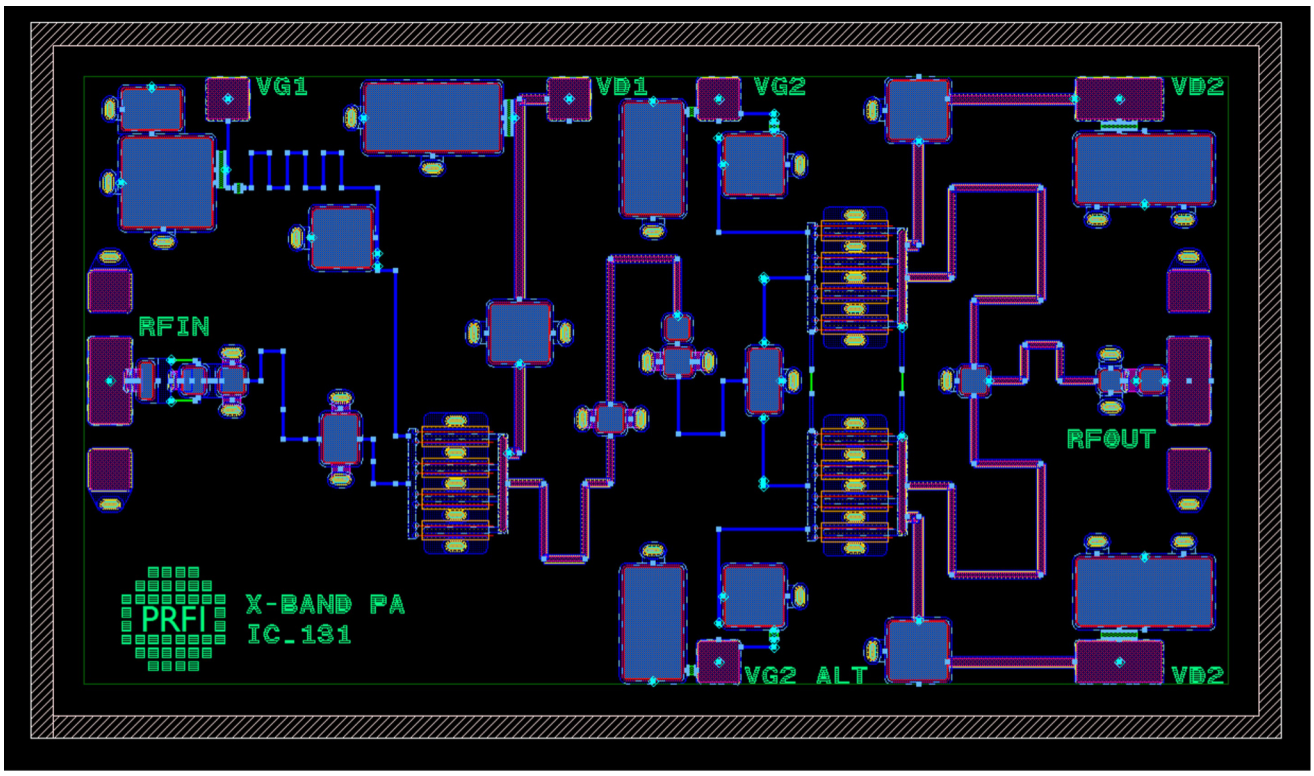

Figure 8: PA layout

Given the high gain of this process, our target of 25dB small signal gain should be achievable using just two stages.

Similarly, we can determine the number and size of the transistors that must be combined in each stage of the amplifier to generate the required power. Our design example uses two transistors in the output stage with their outputs power combined to achieve the 10W output power target.

The size of the driver stage transistor also needs to be carefully considered. Although there is always a lot of attention devoted to the efficiency of the output stage, the driver stage efficiency will also contribute to the overall PA efficiency. If we make the driver stage transistor too large, it will be inefficient and thus will degrade the overall PA efficiency. However, if the driver stage is too small, it will start compressing before the output stage, and will not be able to supply sufficient power to drive the output stage. This would then limit the overall output power of the PA.

Detailed Schematic Design

The PA design is progressed using the selected topology to the point of being fully realised using all PDK component models. Key considerations during the schematic design are matching, biasing, RF power combining/splitting and ensuring broadband unconditional stability.

The matching networks aim to present the desired impedances to the transistors for maximum performance. Shunt inductive elements at the transistor outputs are frequently used to help compensate for the intrinsic drain-source capacitance (C_{DS}), whilst a low pass structure transforms the output impedance. For the power-combined output devices, it is very important to preserve the symmetry of the load that is presented to each output transistor.

The matching networks must also pass gate and drain bias to the transistors. Drain bias is often injected via a shunt matching inductor at its RF short point (capacitor to ground). Gate bias networks include biasing resistance to limit forward gate current whilst avoiding degradation of large signal performance that could occur if the resistors are too large.

The power combining of the output transistors should be integral to the matching network design, as this approach minimises both the die area and associated losses. When multiple power combined transistors are used

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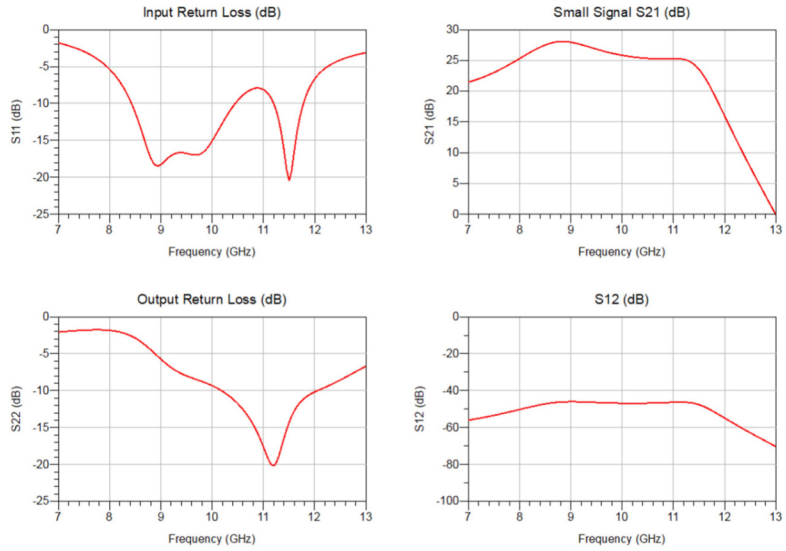

Figure 9: Small signal PA performance

the possibility of odd-mode stability issues arise and loop stability analysis should be performed to identify and resolve any potential issues.

The input resistance added to the transistors in the early stages of the design to ensure unconditional stability can be reduced as the practical losses of PDK matching components are introduced. At microwave and mmWave frequencies additional resistive losses to ensure in-band stability are often unnecessary. Low frequency stability must also be ensured and suitable components can often be added to the gate and drain biasing networks to ensure this. Above band stability must also be ensured up to the F_{max} of the transistors.

Layout

The schematic design must be translated to an MMIC layout for fabrication. This will include the addition of interconnect tracks that may have not been in the schematic simulation as well as proximity and discontinuity effects. These can be accounted for by EM simulation, discussed later. The layout tends to be a compromise between die size and risk. The smaller the die size the lower the cost and the commercial team will push for the smallest possible die size. However, the more compact the design the greater the discontinuities and circuit interactions.

Figure 8 shows a representative layout of the two stage X-band GaN PA under consideration with the RF input to the left and the RF output to the right. Both input and output include Ground-Signal-Ground (GSG) pads to allow RF On Wafer (RFOW testing). The two power combined output transistors can be seen towards the output of the die followed by the matching and power combing network. Odd-mode stabilisation resistors are included between the two output transistors. The single transistor used for the input stage can be seen to the left with its output matching network splitting into two to drive the two output devices. DC-blocking and stabilisation networks are included on chip. The DC and RF pads are all labelled and their function can be easily

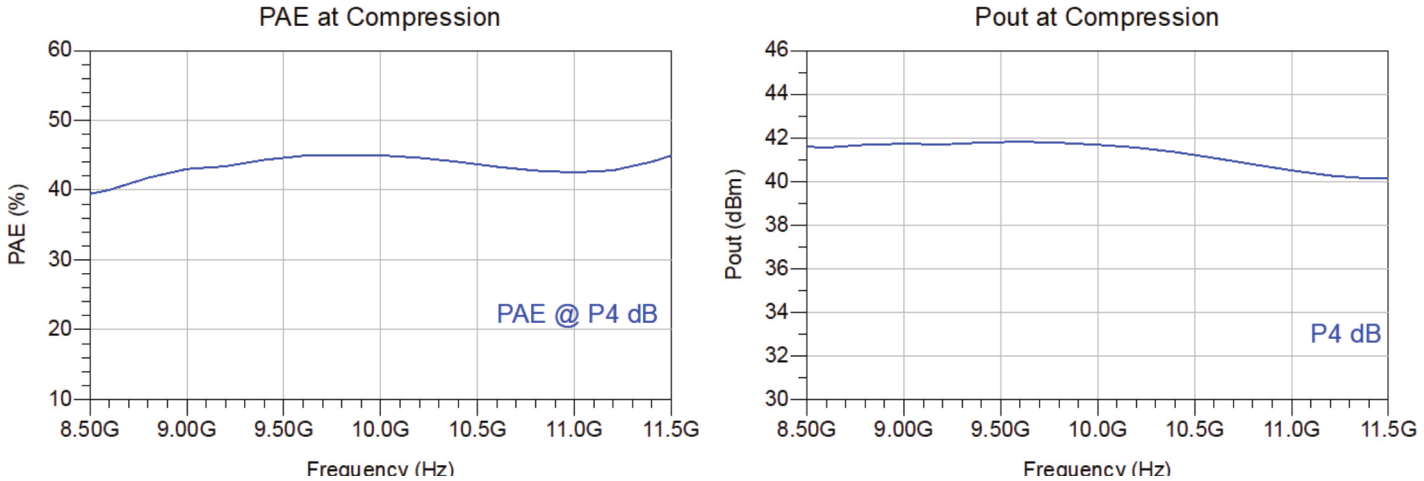

Figure 10: Large signal PA performance

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Parameter	Target	Simulated	Units
Frequency	9.0 – 11.0	9.0 – 11.0	GHz
SS Gain	25	> 25.2	dB
P_{4dB}	40	> 40.5	dBm
	10	> 11.2	W
PAE at P_{4dB}	> 30	> 42.5	%
Input Return Loss	> 10	12 typ.	dB
Operating conditions	28	28	V

Table 3: Phased array radar application

identified. The overall die size is 2.80 x 1.60mm. For components intended for assembly into packages the layout should be optimised with the package in mind and the IC to PCB transitions, including bondwire parasitics, must be simulated and accounted for.

EM Simulation

EM simulation of the MMIC layout is vital to ensure best agreement between modelled and measured performance. The foundry supplies an EM stack-up along with the PDK that allows EM simulation of all passive components to be performed. The PDK transistor models are then added to the EM simulated passive circuitry. It would be a mistake to try and EM simulate the entire structure of a first pass MMIC layout in one go. The best approach is to EM simulate the MMIC a piece at a time, gradually increasing the extent of the EM simulation. The layout and the schematic design can be optimised as the EM simulated network builds up. For PAs the EM network is normally built up from output to input. This is a necessarily iterative process and can be time consuming but it is vital if best performance is to be obtained.

Simulated Results

Figure 9 shows the simulated small-signal performance for the PA with greater than 25dB gain across the intended 9 – 11GHz band with some guard band both above and below band. Input return losses are around 10 – 15dB. As expected for a PA, the output return loss is lower than the input return loss as the output is matched for best large signal performance resulting in a compromise between PAE, output power and gain.

Large-signal simulated performance is shown in Figure 10 and indicates an output power of greater than 40 dBm (10 W) across 8.5 – 11.5GHz and greater than 40.5dBm in the design band. PAE is greater than 42.5% at 4dB compression, which is particularly notable for a two-stage design. Table 3 compares the simulated performance to the original target specification and shows that the target performance is met.

Summary

Active phased-array radar is a key application for X-band power amplifiers and GaN-on-SiC technology has been shown to have several key advantages over other compound semiconductor processes. The G28V5 GaN-on-SiC process from Wolfspeed has inherently high gain which can reduce the required number of gain stages in a radar system line-up and thus simplify the system design and increase PAE. The design of a representative 9 – 11GHz 10W PA has been outlined in this white paper and the simulated performance indicates high output power and PAE across the design band.

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