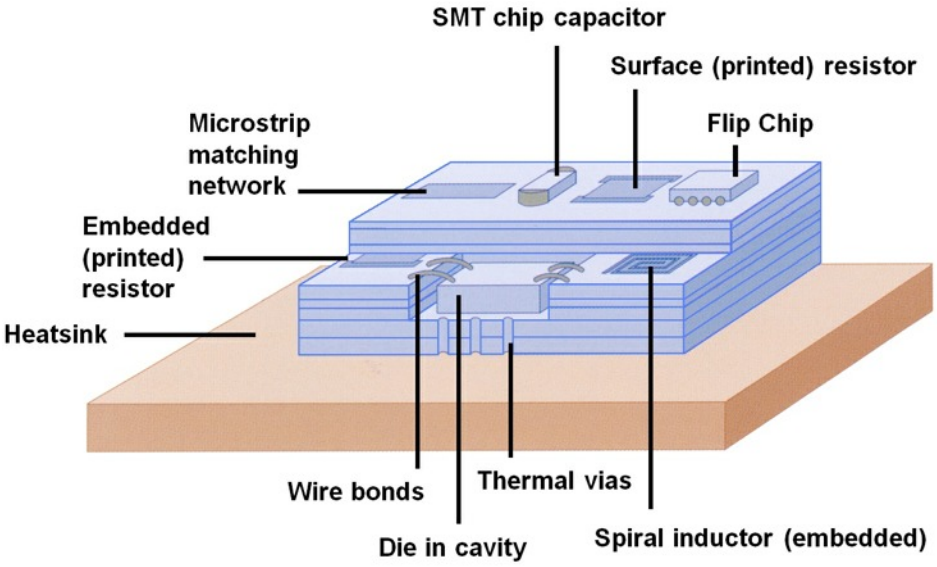
Technology Overview

LTCC

Low Temperature Co-fired Ceramic (LTCC) is a multi-layer ceramic substrate technology that allows the realisation of multiple embedded passive components (Rs, Ls and Cs) in a single, compact, SMT compatible component. Bare die or SMT packaged parts can also be included as an integral part of an LTCC component, which allows the incorporation of multiple technologies to produce high levels of functionality.



LTCC was originally developed from multi-layer capacitor fabrication technology. Fabrication commences with the manufacture of the ceramic material from a mixture of organic and inorganic materials to form a thin flexible tape. At this stage the ceramic substrate material is said to be in its "green state" and is quite fragile. Each LTCC component is fabricated from multiple tape layers processed in parallel (so reducing cost) to form a multi-layer ceramic "sandwich". Different patterning of metals and resistive materials on the separate layers allows the design of complex functionality within the LTCC component.

An example of a typical LTCC process flow is depicted overleaf. Component manufacture commences with the blank green tape ceramic material being cut in to tiles of the required size (typically 100-200mm square). Vias and cavities are then punched in the blank tiles and the vias filled with conductive paste. The required conductor pattern is then printed with conductive pastes (also called "inks"). Resistive inks can also be printed to form integral resistors. These processes are all carried out in parallel for each of the different layers of the LTCC component. Once all of the layers have been completed and checked they are collated in to a stack. They are then laminated under pressure and sintered at around 850°C (a relatively low firing temperature, achieved by mixing glass with the ceramic powder during tape formation or "casting"). The laminated stack is finally sawn and the individual pieces are available for component assembly and test.

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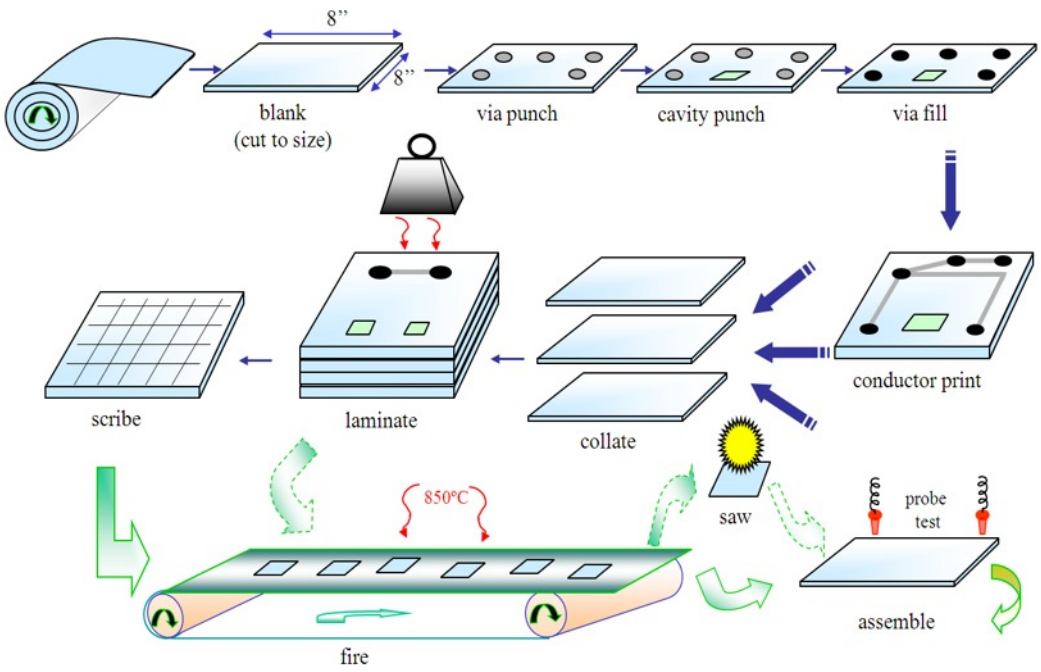

LTCC Tile Manufacture

A range of LTCC substrate materials are available with typical dielectric constants in the range of 6 to 10. High dielectric constant materials are also sometimes used for miniaturisation at lower frequencies or the implementation of higher value capacitors. The thickness of the individual tape layers is typically in the range 100mm-200mm. The maximum number of layers in an LTCC stack is normally around 20-30, with a minimum number of layers being around 6 to 8, to avoid the risk of warping. The total thickness of the LTCC stack is typically 0.8-6mm and the maximum substrate size, of an individual component, is around 100mm square.

LTCC Fabrication Facilities (Foundries)

There are a small number of companies that provide the raw green tape LTCC ceramic materials. These companies also provide the conductive and resistive pastes to be used with their ceramic tapes as compatible "tape systems".

There are a larger number of LTCC companies that process the tape and conductor pastes to produce LTCC products; some of these also have their own in-house tape systems. Whilst some LTCC manufacturers only manufacture their own products, others will also manufacture designs for third parties (an LTCC foundry service). In this case a foundry design guide is usually provided detailing the relevant process limits that must be applied to realise a successful product.

Benefits and Drawbacks of using LTCC

The following are the main benefits of LTCC technology:

- Multi-layer circuitry allows compact implementation
- High dielectric constant reduces distributed component size
- Integration of printed passives (RLC) is possible
- Good control of dielectric properties (thickness and dielectric constant)
- Low loss tangent
- All layers processed in parallel allowing reductions in time and cost
- Well suited to high volume production
- Vias are filled and buried vias easily included
- Good match to semiconductor TCEs
- Good thermal conductivity
- Can tolerate high temperatures, making it well suited for use in harsh environments

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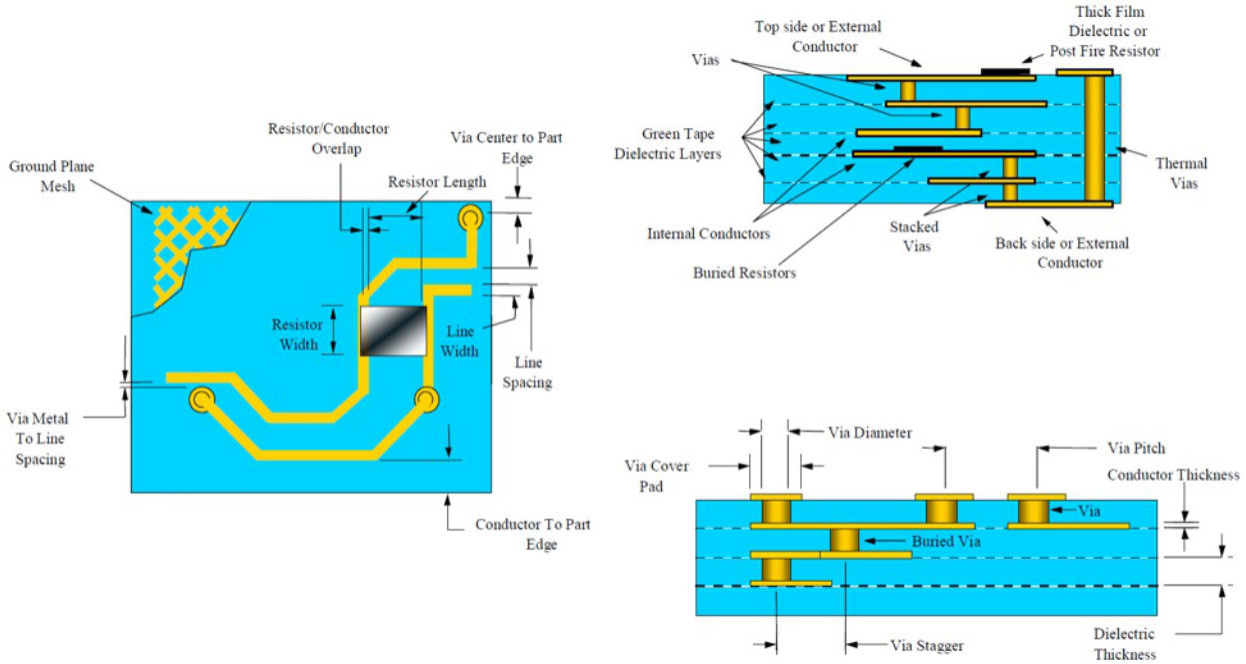

Typical key features detailed in design rules (DuPont)

There are, of course, some limitations to LTCC including:

- Metallisation is screen printed giving limited definition compared to thin-film
- Substrate is not polished and poor surface roughness can result in higher losses
- Care must be taken during the design process to avoid substrate warping
- Processing is more expensive than multi-layer laminate
- Processing lead-times are longer than multi-layer laminate (typically 4-8 weeks)

Typical Design Guidelines and Practical Considerations

Most LTCC foundries provide a summary of their layout guidelines in tabular form. Annotated illustrations accompanying the tables are also used as an effective means of quickly conveying the key features as shown in the example above. Design rules and guides vary from foundry to foundry but in all cases the use of the minimum allowed dimensions throughout should be avoided as this will reduce yield.

Conductor tracks are generally based on either Gold (Au) or Silver (Ag). Different pastes have to be selected to be compatible with either wirebonding and/or soldering. The minimum recommended track width is typically 100-150mm ±25mmand minimum recommended spacing between tracks is typically 100-200 mm ± 25mm. The required distance from track to substrate edge is typically 500mmwhilst the track to cavity edge allowance is typically 300mm.

Large areas of buried metal, such as those for RF ground planes, should be gridded to ensure adhesion of the adjacent tape layers and to provide metal balance avoiding warping of the tile during firing.

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The thick film nature of LTCC limits the achievable metal definition. In an attempt to improve this, modified or additional process steps have been developed to allow better track and gap definition. These include “fine mesh” systems and photoimageable systems. The fine mesh systems simply use a much finer mesh to improve the definition of the printing process. This is possible for all layers but increases cost and fabrication time and the achievable tolerance is still some way from that offered by thin-film techniques.

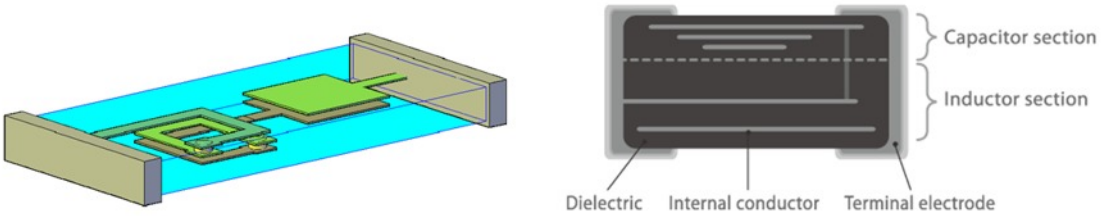
Photoimageable processing is undertaken after firing and is only possible on the surface layers. It essentially uses thick-film printing of conductor on the substrate and then photolithographically defines the required pattern in a manner similar to that used in thin-film processing. This also adds to the processing costs and timescales.

Vias are punched when the tape is in the green state and multiple via diameters can be used in a single component. However, cost increases with the absolute number of vias and with the number of different via diameters.

A typical via diameter is 200mmbut the value is somewhat dependent upon the tape thickness. Other production requirements define via to via spacing, via to edge separation, minimum catch pad size and catch pad to track separation.

Cross-sectional images of vias provided by LTCC foundries as examples of their work can convey the impression that stacked vias produce well formed tubular columns. However, practical limitations such as layer registration error, punch shape, via fill and shrinkage in the process introduce uncertainties. Most foundries actually discourage the use of vertical via stacks recommending that vias be staggered on adjacent layers to minimise the above effects. This can complicate the design, simulation and layout process and makes the realisation of compact LTCC circuits more challenging. Several other requirements, including spacing between vias, via catch pad dimensions and via proximity to tracking, tile edges and cavities all increase the challenge of realising compact LTCC components.

Resistors can be included in LTCC components by printing an additional resistive ink as part of the processing. The length and width are both limited to a minimum of about 0.38mm. Resistors can be printed on any tape layer so it is straightforward to include buried resistors within the LTCC stack-up. Sheet resistivity values available vary between about 10Ω/square and 10kΩ/square with a tolerance of ±30%. This tolerance value limits the usefulness of embedded LTCC resistors. If the resistors are realised on the surface it is then possible to laser trim to provide a tolerance of about ±2%. It is also noted that not all resistive inks are suitable for buried structures.



Lumped LTCC series LC filters - linear & stacked (Syfer & TDK)

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Capacitors can be formed as printed structures using a pair of overlapping plates on either side of a single dielectric layer. Multiple overlapping plates can be used on several layers (similar to the structure of conventional multi-layer capacitors) to increase the area and thus the capacitance value. It is noted that the layer registration needs to be considered when designing a capacitor as this will affect the final value. Typical layer registration tolerances are ±50mm so that the value of smaller capacitors will be affected the most.

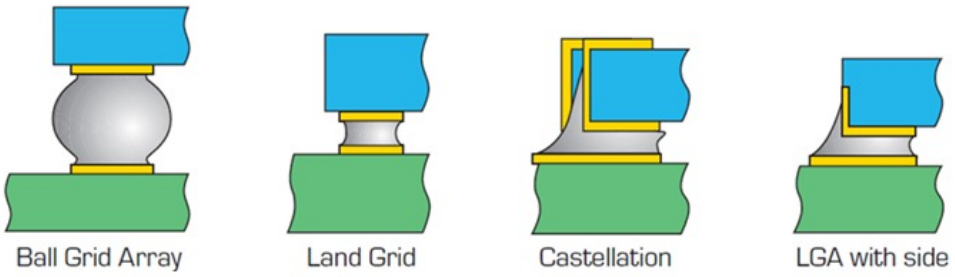
It has been demonstrated that higher dielectric constant material layers can be incorporated in to the LTCC stack-up allowing higher value capacitors to be realised. However, this is not offered by all foundries and would increase the cost of the product.

Inductors can be realised as printed spirals, either as a single layer spiral or multi-layer helical spirals. The multi-layer helical spiral is more space efficient and is the structure typically used in commercially available RF filter products realised in LTCC.

RF filters realised in LTCC are commercially available and normally make use of embedded inductors and capacitors. The image above depicts a series LC filter (left) with the two elements arranged side by side and a series LC filter (right) with the two elements arranged on top of each other which can help in size reduction.

In order to allow LTCC components to interface to the outside world a range of transition types are commonly used, as depicted below. At lower frequencies the method of transitioning from the top-side of a component to the underside, where the component is mounted on the 'motherboard', is generally accomplished with a castellated edge transition. The effect of any excess inductance is essentially negligible at these lower frequencies.

Higher frequency parts often use the LGA (Land Grid Array) interconnect, which utilises vias, rather than castellations, to minimise interface parasitics. At even higher frequencies the inductance of such transitions can start to limit the performance. One method adopted to avoid performance degradation is to essentially form a coaxial transition using a via as the centre conductor and a via fence as the outer coaxial ground.



Examples of LTCC to PCB interconnects (DT Microcircuits)

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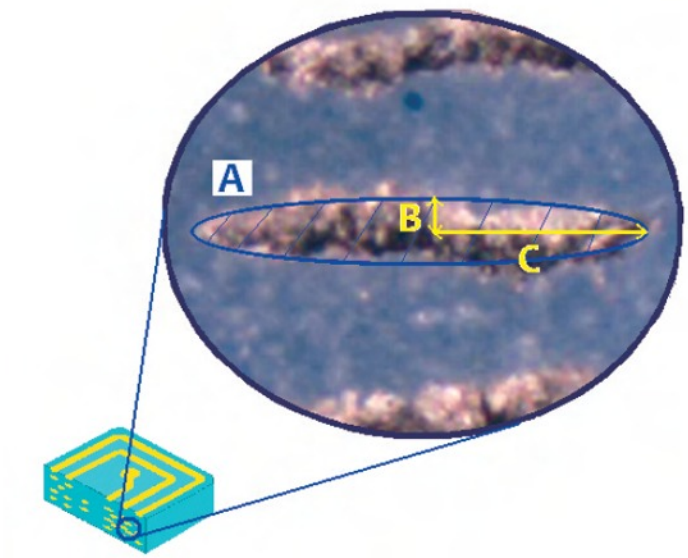
Recommendations and Advice for the Successful Design of LTCC Components

LTCC can be a useful technology for the implementation of compact RF and microwave components. However, it does have its limitations and any oversights during the design process can greatly increase the cost and reduce the performance of the resulting components. The following practical points are offered for consideration:

- Keep the design as simple as possible
- Whenever possible keep well away from design rule limits
- LTCC is a thick film process so the achievable metal definition is limited – allow for this and make sure the design can tolerate expected variation
- The minimum track and gap rules can restrict achievable circuit density - don't try to compact the circuitry too much by using minimum design rules throughout
- Via holes also have a strong effect on achievable circuit density and this should be considered from the outset:
  - Vias are punched and thus relatively large (comparable to the tape thickness)
  - Relatively large catch pads are required for each via
  - Via proximity rules can have a significant effect
- The tape deforms around the conductor resulting in a nominally elliptical cross-section which is difficult to simulate accurately (as shown in the image below)
- Metal balance should be maintained to avoid warping – use gridded ground-planes
- Too few tape layers can result in warping (~6 layers minimum, preferably 8 or more)
- Although cavities can be included they add numerous design complications and are usually avoided whenever practical



Cross-section of embedded LTCC line (Anaren)

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